Journal of Astronomical Telescopes, Instruments, and Systems

AstronomicalTelescopes.SPIEDigitalLibrary.org

Progress of coating stress compensation of silicon mirrors for Lynx x-ray telescope mission concept using thermal oxide patterning method

Youwei Yao
Brandon D. Chalifoux
Ralf K. Heilmann
Kai-Wing Chan
Hideyuki Mori
Takashi Okajima
William W. Zhang
Mark L. Schattenburg

SPIE.

Youwei Yao, Brandon D. Chalifoux, Ralf K. Heilmann, Kai-Wing Chan, Hideyuki Mori, Takashi Okajima, William W. Zhang, Mark L. Schattenburg, "Progress of coating stress compensation of silicon mirrors for Lynx x-ray telescope mission concept using thermal oxide patterning method," *J. Astron. Telesc. Instrum. Syst.* **5**(2), 021011 (2019), doi: 10.1117/1.JATIS.5.2.021011.

Progress of coating stress compensation of silicon mirrors for Lynx x-ray telescope mission concept using thermal oxide patterning method

Youwei Yao,[a,*] Brandon D. Chalifoux,[a,b] Ralf K. Heilmann,[a] Kai-Wing Chan,[c,d] Hideyuki Mori,[c,d] Takashi Okajima,[c] William W. Zhang,[c] and Mark L. Schattenburg[a]
[a]MIT Kavli Institute for Astrophysics and Space Research, Space Nanotechnology Laboratory, Cambridge, Massachusetts, United States
[b]MIT, Department of Mechanical Engineering, Cambridge, Massachusetts, United States
[c]NASA Goddard Space Flight Center, Greenbelt, Maryland, United States
[d]University of Maryland-Baltimore County, Baltimore, Maryland, United States

Abstract. A thermal oxide patterning method has proven to be effective for correcting coating-stress-induced distortion on flat silicon wafers. We report progress on developing this method for correcting curved silicon mirrors distorted by front-side iridium coatings. Owing to the difference in geometry, a finite element model has been established to calculate the appropriate duty cycle maps in thermal oxide hexagon patterns used for compensation. In addition, a photolithographic process, along with three-dimensional printed equipment, has been developed for creating patterns precisely on the back side of curved mirrors. The developed method has been used to recover the original surface shape of two silicon mirrors which are 100-mm long, 0.5-mm thick, having 312-mm radius of curvature, and 30 deg in azimuthal span (Wolter-I geometry). These mirrors' front sides are sputter-coated by 20-nm iridium layers with ~-70 N/m integrated stress. Measurement results show that the developed method can mitigate coating-induced distortion by a factor of ~5 in RMS height and ~4 in RMS slope error, corresponding to ~0.5 arc sec RMS slope error. Residual errors after correction are dominated by mid-frequency ripples created during the annealing process, which will be resolved in the future. The presented method is precise and inexpensive and a potential candidate for resolving the coating stress issue for Lynx optics in the future. [DOI: 10.1117/1.JATIS.5.2.021011]

Keywords: x-ray; silicon mirror; thermal oxide pattern; figure correction; coating stress; stability.

Paper 18101SS received Nov. 1, 2018; accepted for publication Apr. 8, 2019; published online Apr. 29, 2019.

1 Introduction

NASA's next-generation flagship x-ray telescope concept, called Lynx, is currently under study for consideration by the 2020 Astrophysics Decadal Review.[1] The mission concept calls for a similar angular resolution as Chandra (0.5 arc sec half-power diameter), but with a much higher effective area (30×) and wider field of view.[2] These ambitious goals automatically lead to a light-weighted mirror strategy, as has been demonstrated by NuSTAR's hot slumping mirrors,[3] but requiring ~100× better surface figure quality. In the past several years, a group at the NASA Goddard Space Flight Center (GSFC) has developed a technology for producing low-cost silicon meta-shell mirrors with ~0.5 arc sec RMS slope error.[4] Owing to the intrinsic properties of monocrystalline silicon, which has very low internal stress, these mirrors can be thinned to 0.5 mm without figure degradation on the polished side. Mirror surface quality is still undergoing rapid improvements toward meeting Lynx requirements.

The effective area of mirrors in the x-ray band (0.1 to 10 keV) relies on the performance of reflective coatings. A high-quality coating utilizing high density and low surface roughness increases the critical angle at a fixed photon energy or increases the critical energy at a fixed grazing angle, thereby benefiting the telescope's throughput.[5] Sputtered iridium coatings had been preferred for Chandra's thick full-shell mirrors due to their high performance and good stability. Unfortunately, these coatings have high compressive stress,[6] which will distort thin segmented silicon mirrors far beyond Lynx tolerances.

A number of solutions for mitigating coating-induced distortion in thin x-ray mirrors have been investigated by several groups. Technologies can be summarized and divided into two kinds. The first kind minimized the coating distortion by reducing the front-side coating stress. A group at NASA Marshall Space Flight Center, by measuring the wafer curvature *in situ* and controlling the working gas pressure, was able to deposit a 15-nm-thick iridium layer on a 2-inch diameter flat wafer with stress around 3 MPa (0.05 N/m),[7] which may be low enough for Lynx.[8] However, the coating stress uniformity, stability, and reflectivity are critical and have not yet been demonstrated. Another group at GSFC tried to balance the compressive stress in iridium films by depositing a chromium layer with tensile stress underneath the iridium.[9] They also attempted to reduce the compressive stress in iridium layers by annealing at 350°C.[6] Neither of these methods alleviated the mirror sag error to better than 1 to 2 arc sec.

The second kind of technology compensated iridium stress by coating a layer with compressive stress on the back side of the mirrors. Methods using atomic layer deposition,[9] ion implantation,[10] sputtering iridium layers with optimized thickness,[11] chromium layers with manipulated bias voltage,[12] and PZT active correction[13] were attempted by multiple groups and have achieved limited success, but a general robust method has not yet been demonstrated.

*Address all correspondence to Youwei Yao, E-mail: yaoyw@mit.edu

The thermal oxide patterning method[14,15] developed by our group has demonstrated a capability of compensating coating stress distortion on flat silicon wafers with high precision and good stability, which could potentially benefit x-ray mirrors with high coating quality and excellent surface shape. Since the size of the oxide patterns on the back side of the mirror is relatively large (0.5 mm), the method has potential for low-cost mass production. In this paper, we report progress of extending this method to GSFC's curved silicon mirrors.

2 Process

In this paper we demonstrate the thermal oxide patterning method for compensating coating stress on two pieces of curved silicon mirrors. The mirror geometry is as follows: 100-mm long, 0.5-mm thick, 312-mm radius of curvature, and 30 deg in azimuthal span (Wolter-I geometry). Mirror front sides are coated with 20-nm-thick iridium layers with ~-70 N/m integrated stress. Chromium layers of 3-nm thickness were first sputtered before the iridium to (1) improve adhesion and (2) reduce the overall stress after coating. The mirrors were fabricated, coated, and measured at GSFC. The thermal oxide patterns were designed and produced on mirror back sides at MIT.

The process flow is shown in Fig. 1. In step 1, the fabricated mirrors are oxidized at 1050°C for 3 h to grow ~200 nm thermal SiO_2 layers on both sides of the mirrors. This process produces ~-70 N/m integrated stress in the thermal oxide, which can be used in later steps to compensate for iridium coating stress. The thickness of the oxide could be adjusted for different coating stress. After oxidation, in step 2, the mirror front side is measured by a metrology tool at GSFC, which is an interferometer with a cylindrical null.[16] We have found that the measured surface figure before and after oxidation is unchanged (within 10 nm in RMS height), indicating the integrated stress field in the back side oxide is the same as that on the front side. The

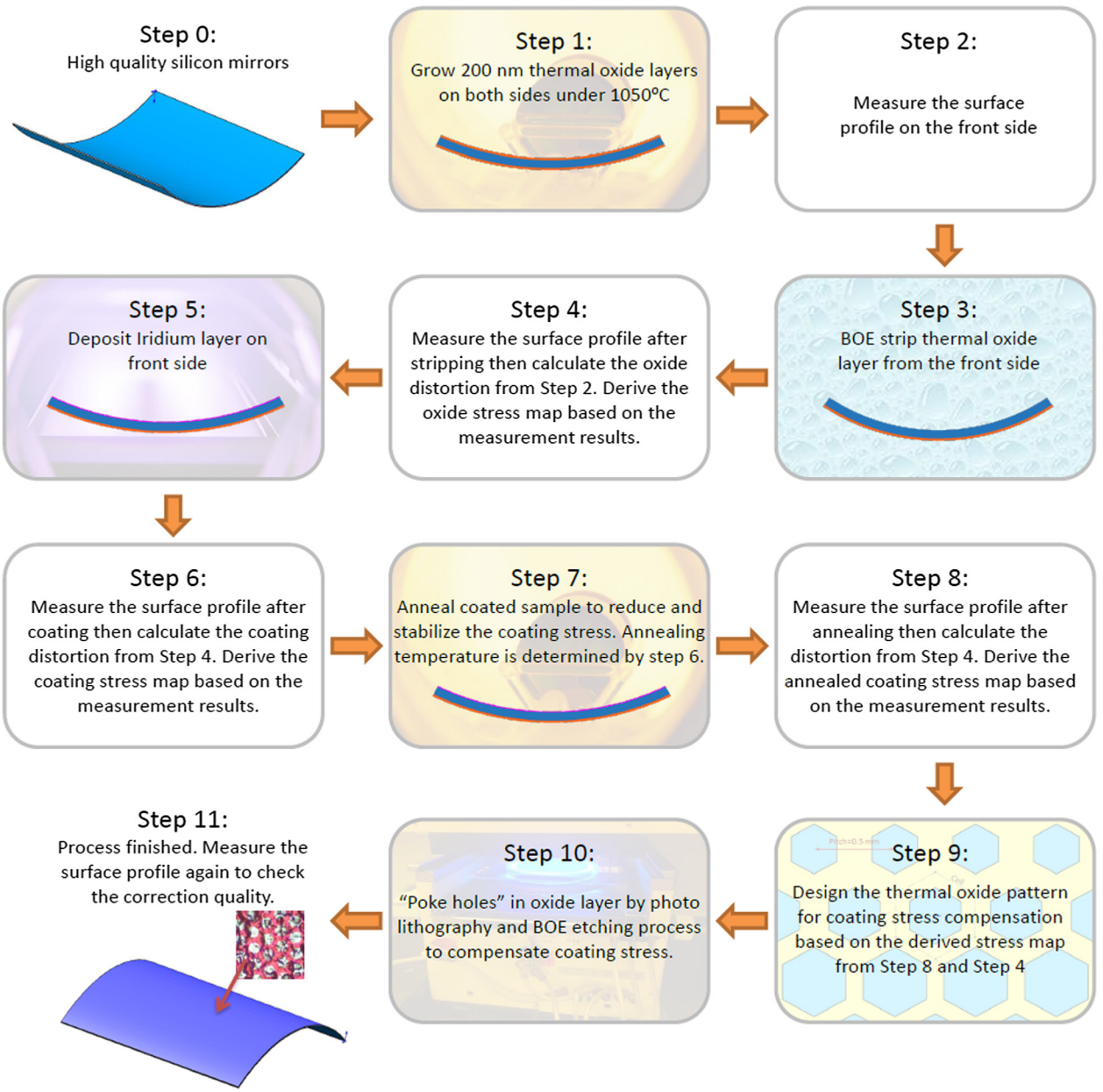


Fig. 1 Process flow of coating stress compensation for curved silicon mirrors.

surface topology map M_1 measured in step 2 is used as the mirror's initial figure.

In step 3, the mirror back side is spin-coated with Dow SPR-700 photoresist (PR) by using our curved mirror spin tool (CMST) (see Sec. 2.4) and baked on a hotplate at 110°C for 3 min. Then the mirror is dipped into 1:7 buffered oxide etch (BOE) for 5 min to remove the front-side oxide. The back-side PR layer is subsequently removed in piranha etch solution.

In step 4, the surface topology map of the mirror back-side oxide, M_2, is measured by the metrology tool. The stress map of the oxide layer is calculated from the deformation map $M_2 - M_1$. The stress map calculation is based on our finite element (FE) model (see Sec. 2.1).

In step 5, the mirror front side is coated first with a 3-nm chromium layer to promote adhesion and a 20-nm iridium layer for x-ray reflection. The average integrated stress in the coating is ~-70 N/m. This step is accomplished by a DC magnetron sputtering system at GSFC. After coating, the surface topology of the mirror M_3 is measured in step 6 to calculate the coating-induced distortion, $M_3 - M_2$, thereby deriving a coating stress map as a reference for the following annealing process.

In step 7, the coated mirror is annealed in a tube furnace for 2 h (Sec. 2.2). The annealing temperature is determined carefully to ensure that (1) the coating stress after annealing is slightly lower that the oxide stress and (2) the surface roughness does not degrade. After annealing, in step 8, the mirror topology is again measured as M_4 to determine the mirror distortion induced by annealed coating, which is $M_4 - M_2$. The stress map of the annealed coating is thus derived.

Based on the calculated stress maps of the annealed coating and thermal oxide layers, in step 9, a hexagon pattern in the thermal oxide layer is designed to precisely balance the coating stress (Sec. 2.3). The pattern is an array of hexagon voids with fixed pitch (0.5 mm) and variable duty cycle. The pattern geometry and the design process are the same as we applied on flat silicon wafers.[14,15]

In step 10, the designed patterns are fabricated in the thermal oxide layer on curved surfaces by using a customized photolithographic process (see Sec. 2.3). In the last step 11, the front surface topology of the back-side patterned mirrors are again measured to confirm the quality of coating stress compensation.

2.1 *Metrology and Stress Calculation*

The design of the hexagon pattern is derived from the measured stress maps of the annealed iridium coating and thermal oxide layers, which are calculated from the measured surface topologies. Therefore, surface metrology is of crucial importance. In this work, the measurements of the mirror surfaces are accomplished by an interferometer with a cylindrical null at GSFC. The 100 mm × 30 deg mirror surfaces are covered by ~420 × 175 pixels which corresponds to ~0.25 mm × ~0.17 deg per pixel. Each column of the measured data (along axial direction) is fitted by 31 terms of Legendre polynomials. The zeroth and first Legendre orders, which represent piston and tilt of the axial profiles, are removed to eliminate defocusing errors in measurements. The fits without those two terms are used as the surface topography. Figure 2(a) shows an example, which is the measured surface distortion induced by back-side oxide on mirror 312S1024.

By using measured distortions, stress maps in the thermal oxide and iridium layers are calculated by using an FE model established in the commercial software ADINA. The calculation is based on a pseudoinverse method, which is similar to the one we established for flat wafers.[14,15] Based on the assumption that the stress maps are dominated by low-frequency components, in our model the stress is represented by a two-dimensional Legendre polynomial which has nine terms (the first three orders for two directions produce 3^2 terms). Figure 2(b) shows a calculated stress map in the thermal oxide layer based on the measured distortion.

The calculated stress distribution in oxide varies by ~50%, due perhaps to multiple reasons: (1) compared with a flat

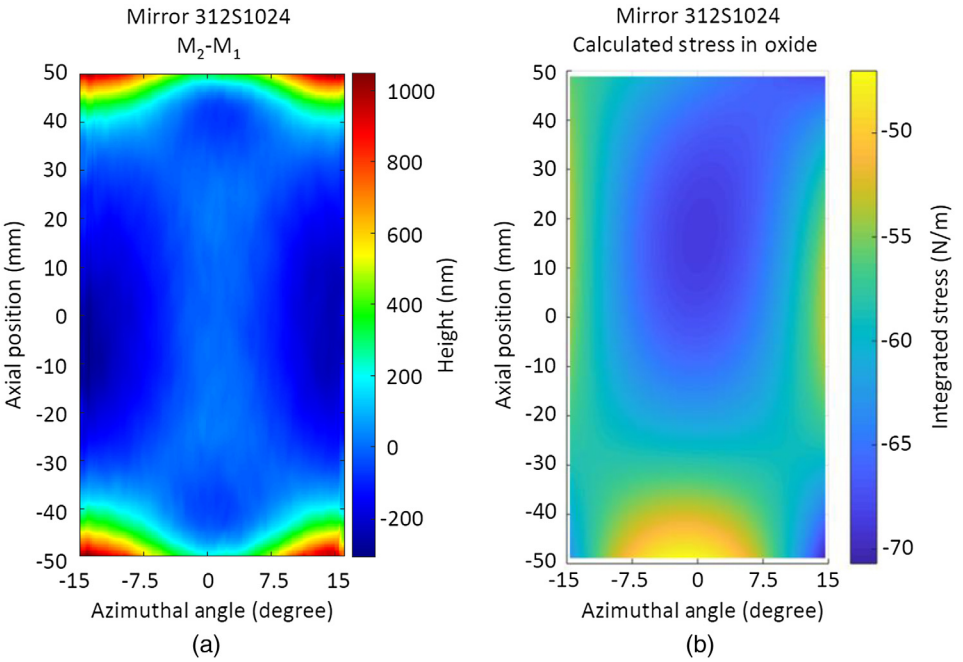


Fig. 2 (a) Measured surface distortion induced by the back-side oxide layer. (b) Calculated stress distribution based on the distortion map shown in (a).

substrate, the deformation of a curved mirror is less sensitive to the coating stress (at least in the axial direction), therefore, small measurement errors in surface topology may lead to a high variation in calculated stress and (2) nonuniformity of the thickness or crystal orientation in curved silicon mirrors may result in deviation in stress calculation.

2.2 *Annealing Process for Reflective Coatings*

The photolithographic process for creating PR patterns requires baking the coated mirror at ~110°C, which can potentially relax the stress in the chromium and iridium films and cause large compensation errors. Therefore, the mirrors are annealed after sputtering at a higher temperature to relax and stabilize the stress. Since the thermal oxide patterning method compensates the coating stress by means of the stress in the oxide, and the coating stress can vary due to the sputtering conditions, sometimes the coating stress may be higher than the oxide stress, which will jeopardize the stress compensation. An annealing process with appropriate temperature after deposition can reduce the coating stress to within the capture range.

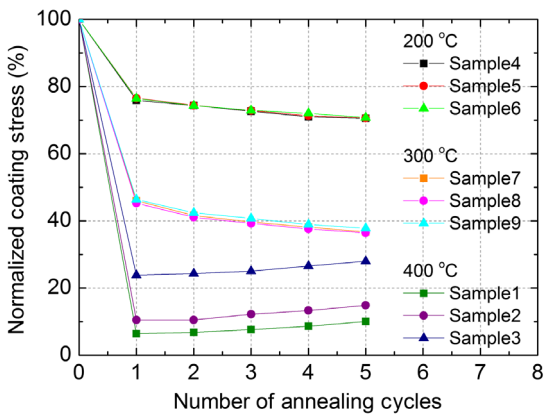


Fig. 3 Measured residual stress in 20-nm-thick iridium layers versus number of 2-h thermal cycles for 200°C, 300°C, and 400°C.

To demonstrate effective annealing, we coated nine flat silicon wafers with 20-nm iridium, annealed them under different temperatures, and tracked the stress relaxation for multiple thermal cycles, as shown in Fig. 3. Since we did not find adhesion problems on those wafers, there was no adhesive interlayer between iridium coatings and silicon wafers. This methodology for chromium-coated flat wafers has already been demonstrated in Refs. 14 and 15.

For these annealing cycles most of the stress is relaxed and stabilized in the first cycle, which indicates that an annealing time of 2 h is appropriate. The remaining residual stresses after the first cycle for 200°C and 300°C are ~75% and ~45% of the stress just after coating, respectively. When the temperature is 400°C, the relaxed stress values are scattered, which may be due to random crystallization in the iridium film, suggesting that the annealing temperature is preferred to be lower than 300°C. In addition, the surface roughness of iridium coating does not degrade under 350°C, as has been indicated in Ref. 9. These results help in determining the optimum annealing temperature based on the stress in iridium and thermal oxide. Figure 4 shows measured results for mirror 312S1024, which is the calculated stress map of the iridium coating before and after annealing at 250°C.

Since, for mirror 312S1024, the iridium coating stress is near the same level of the thermal oxide stress, as shown in Fig. 2(b), the annealing temperature is determined to be 250°C. The stress relaxation is ~40% as predicted in Fig. 3. The stress distribution in the coating before and after annealing is similar to the distribution in thermal oxide, which may be due to systematic measurement or stress calculation artifacts that should cancel in the duty cycle calculation, as is demonstrated in the next section.

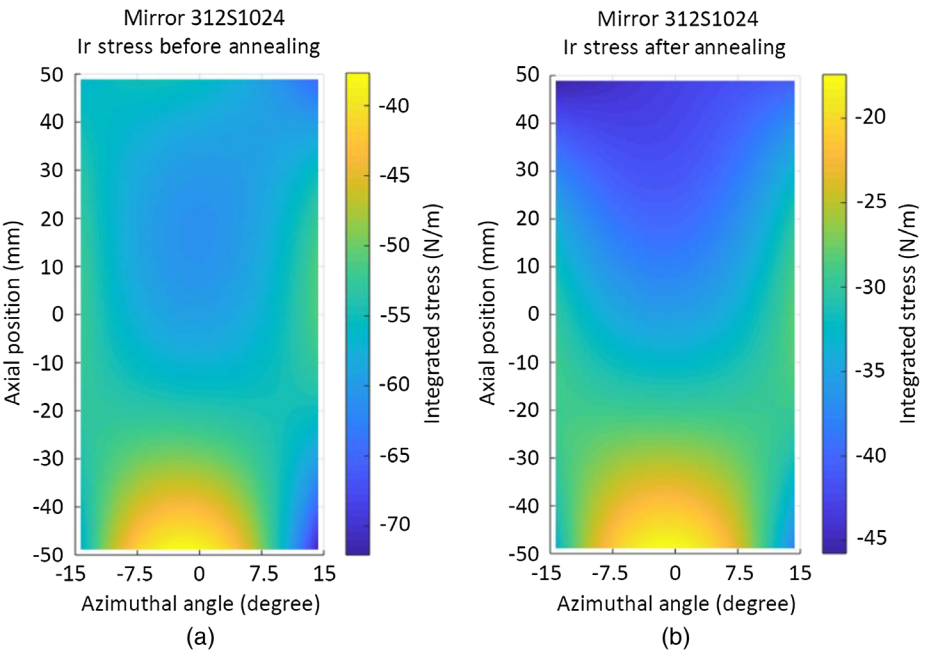


Fig. 4 Stress of a 3-nm chromium + 20-nm iridium coating before (a) and after annealing (b). Note: the scales are different.

2.3 *Pattern Design*

As has been demonstrated in our previous work, the thermal oxide pattern is an array of hexagon-shaped voids with adjustable size in each cell.[14,15] Since the pitch between the hexagons is fixed at 0.5 mm, the area fraction of the hexagon void relative to its unit cell is defined as a duty cycle, which can be calculated by the following equation:

$$\text{Duty cycle}(\theta, Y) = \frac{S_{\text{oxide}}(\theta, Y) - S_{\text{annealed}}(\theta, Y)}{S_{\text{oxide}}(\theta, Y)}, \quad (1)$$

where θ is the coordinate in the azimuthal direction and Y is the axial location. Here, $S_{\text{oxide}}(\theta, Y)$ is the measured stress in thermal oxide, corresponding to Fig. 2(b), and $S_{\text{annealed}}(\theta, Y)$ is the annealed coating stress, corresponding to Fig. 4(b). The calculated duty cycle map based on those two figures is shown in Fig. 5.

The derived duty cycle map is converted to a hexagon plot and saved as an AutoCAD R12 file for the photomask vendor. A plastic film mask is selected for producing the hexagon pattern, which will be discussed in next section.

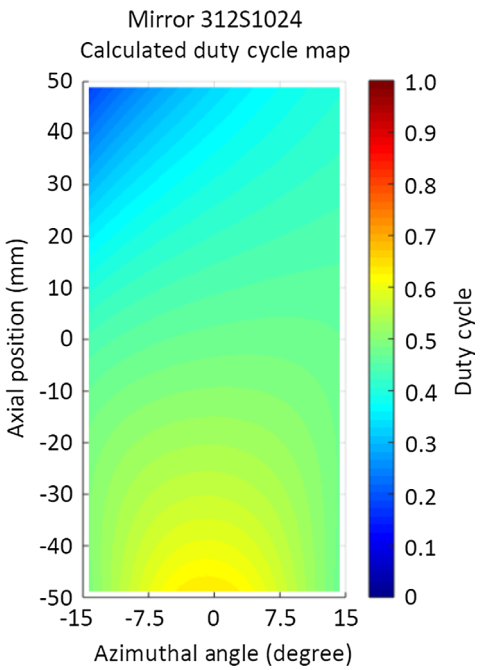
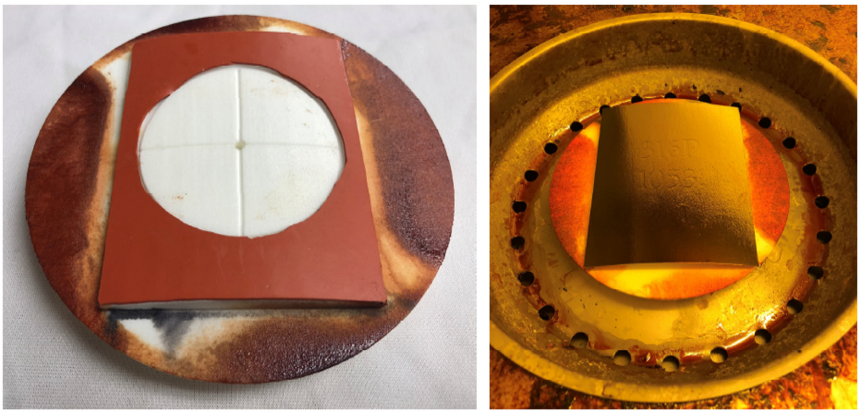


Fig. 5 Example of a duty cycle map derived from Fig. 4(b) and Fig. 2(b).

2.4 *Photo Lithography Process on Curved Mirrors*

A great challenge of this work is to produce the designed pattern on a rough-and-curved silicon surface with good precision. In addition, the roughness of iridium coating on the front side should not degrade through the process. After much trial and error, the fabrication process was eventually matured and is described as follows:

1. Manually paint MicroChemicals AZ-5214 PR on the front side of the mirror and bake the mirror on a hotplate under 110°C for 5 min. Since the iridium coating is covered by a harden PR layer, it is prevented from the following mechanical and chemical exposure to avoid roughness degradation.
2. Place the mirror (facing down) on the CMST (Fig. 6) and carefully align it to the center. Apply vacuum to the mirror to constrain it tightly on the CMST. Spin-coat Dow SPR-700 PR on the back side of the mirror. The RPM is set at 3000, which produces a uniform ~1 μm PR layer on the back side. The spin-coated mirror is baked on a hotplate for 5 min to harden the PR.
3. Place the mirror on a curved mirror exposure tool (CMET, Fig. 7). Press a plastic film mask with the designed hexagon pattern over the mirror, carefully align the mask with the mirror, and fix it with tape. Then cover the mask and the mirror with a plastic vacuum bag. Seal the bag with sticky rubber at the edge of the CMET. Pull a vacuum on the CMET; due to the designed channels, the vacuum bag can press the mask



(a) (b)

Fig. 6 (a) CMST. The white part is a three-dimensional printed plastic chuck which has a curved top surface to match the mirror curvature. The red piece on the top of the plastic is a rubber sheet for sealing. The cross slot with a hole at the center is a vacuum channel. (b) Silicon mirror mounted on the CMST which is coupled with a spin coater. The mirror is spin-coated with DOW SPR-700 PR.

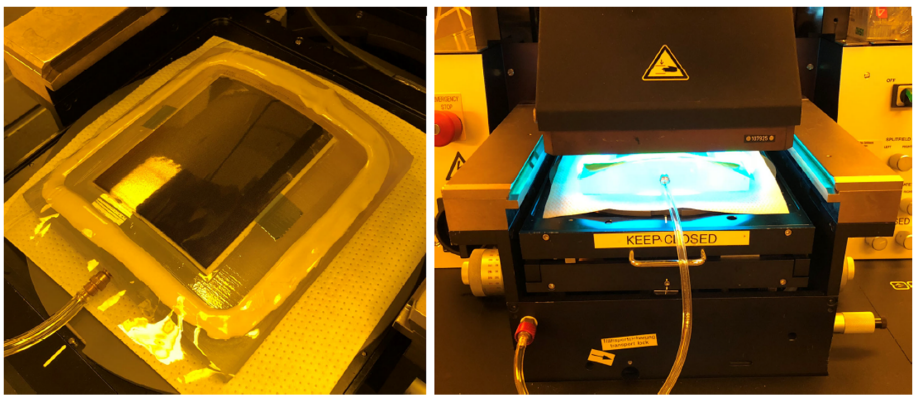
tightly on the back side of the mirror to ensure high precision of pattern transfer.

4. Exposure with UV light (365- and 406-nm wavelengths) for seven cycles. The exposure time for each cycle is 60 s, which leads to 420-s exposure time in total, corresponding to a dose of 3780 mJ/cm^2.
5. Remove the mirror and immerse in developer solution (Microposit MF CD-26) for 90 s. Rinse it in deionized water and blow dry in N_2. This results in a PR layer with hexagon voids patterned on the top of the thermal oxide.
6. Dip the mirror in a BOE solution for 5 min so the thermal oxide within the hexagon voids is thoroughly removed.
7. Soak the mirror in acetone and isopropyl alcohol to strip the PR from both sides of the mirror. Blow dry it in N_2.

After these steps, a thermal oxide pattern remains, as shown in Fig. 8.

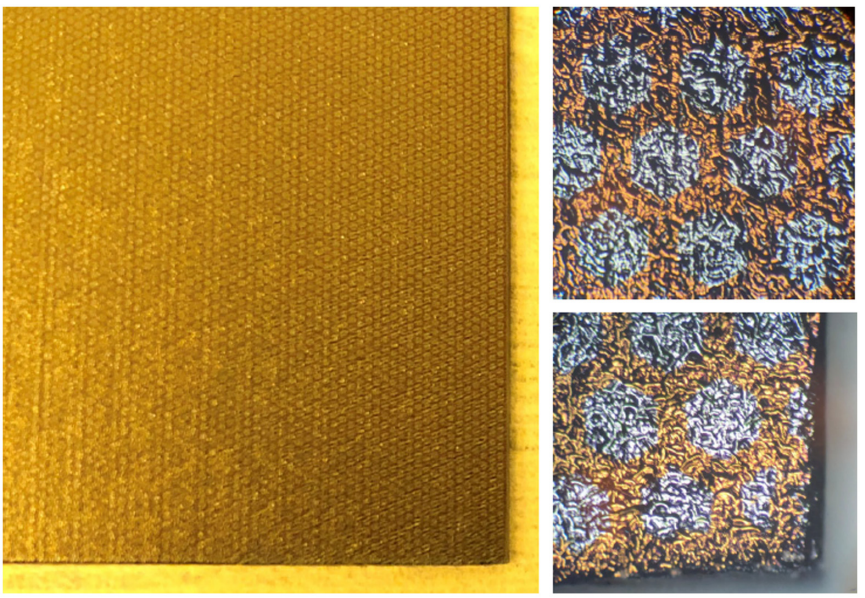
3 Results

The process was applied to two mirrors, 312S1024 and 312P1052, to compensate for the surface distortion induced by 20-nm iridium coatings. Figure 9 shows the measured deformation from the iridium coating (left) and after compensation (right). Table 1 lists the calculated RMS heights and slope errors from these results. The thermal oxide patterning method successfully reduced the coating stress-induced distortion by a



(a) (b)

Fig. 7 (a) CMET with mirror, plastic mask, and a vacuum air bag layers on the top. The tool is a three-dimensional printed plastic mold with embedded vacuum channel. The white ring near the edge is the sticky rubber seal. (b) The assembly under UV exposure.



(a) (b)

Fig. 8 (a) Back side of mirror 312S1024 after patterning. The thermal oxide pattern is visible to the naked eye. (b) Thermal oxide hexagon patterns observed under a microscope. The pattern quality is consistent at mirror center (right-top) and at a corner (right-bottom).

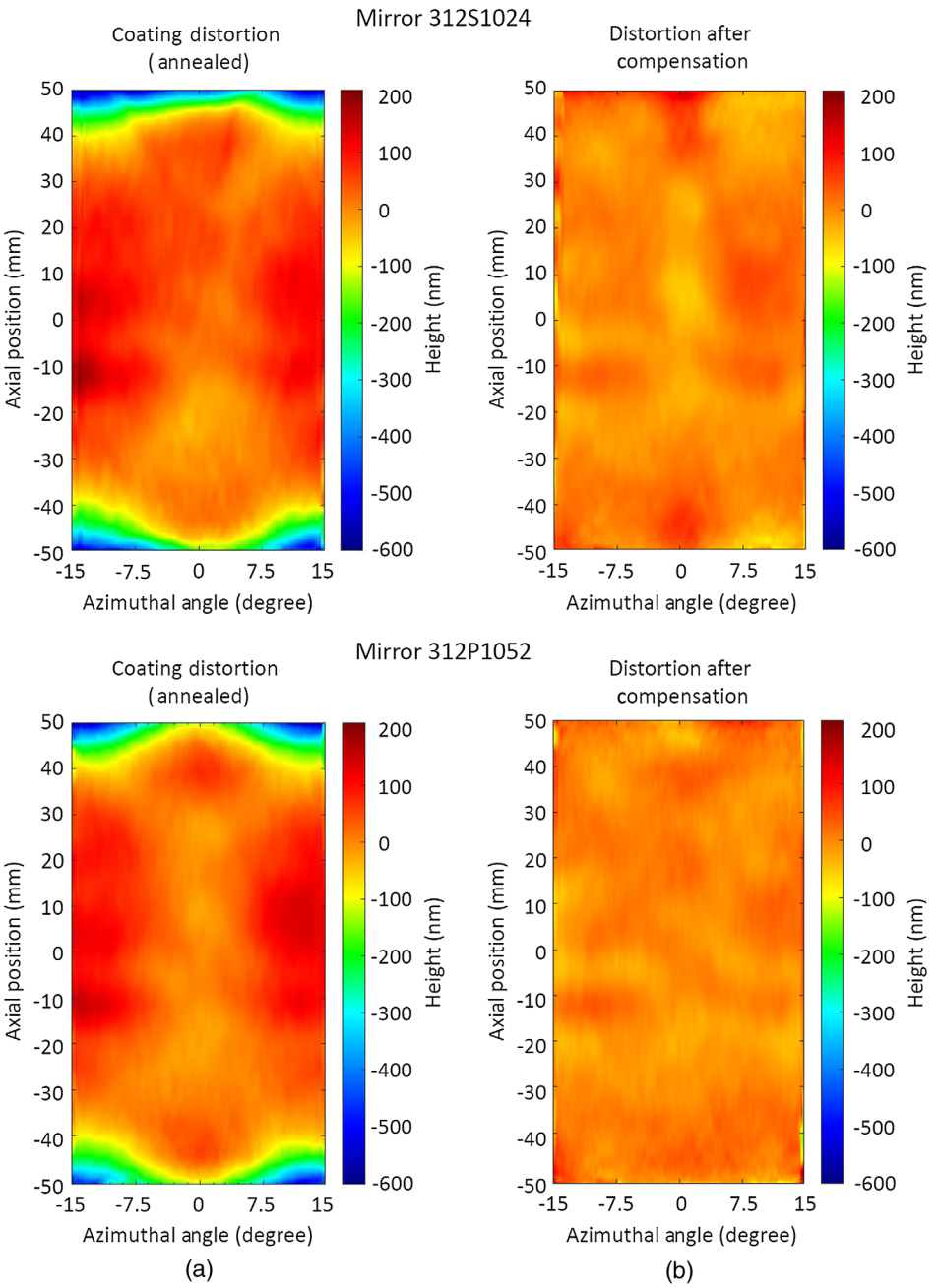


Fig. 9 Measured surface distortion induced by coating (a) after annealing and (b) after stress compensation. For mirror 312S1024, the initial oxide stress is shown in Fig. 2, the coating stress is shown in Fig. 4, the calculated duty cycle is shown in Fig. 5, and the created pattern is shown in Fig. 8.

Table 1 RMS heights and slope errors of coating distortions calculated from Fig. 9.

	RMS height (nm)		RMS slope error (arc sec)	
	Coating distort.	After Comp.	Coating distort.	After Comp.
312S1024	113.7	24.6	1.895	0.504
312P1052	101.2	19.3	1.801	0.484

factor of ~5 in RMS height and ~4 in RMS slope error on those mirrors, which is less than we achieved on flat wafers (~68 in RMS height and ~50 in RMS slope error).

After a close look at the data, we discovered that the residual errors on these mirrors after compensation are dominated by centimeter-scale ripples. Figure 10 shows the measured surface deformation of mirror 312S1024 in steps 2, 6, 8, and 11 relative to the initial shape before oxidation (step 0), where the data are fit by Legendre polynomials, and low frequency terms from zeroth to fourth order are excluded from the plots. The results clearly show that the mid-frequency ripples appeared after the step 7 annealing process and remained after correction in Step 11.

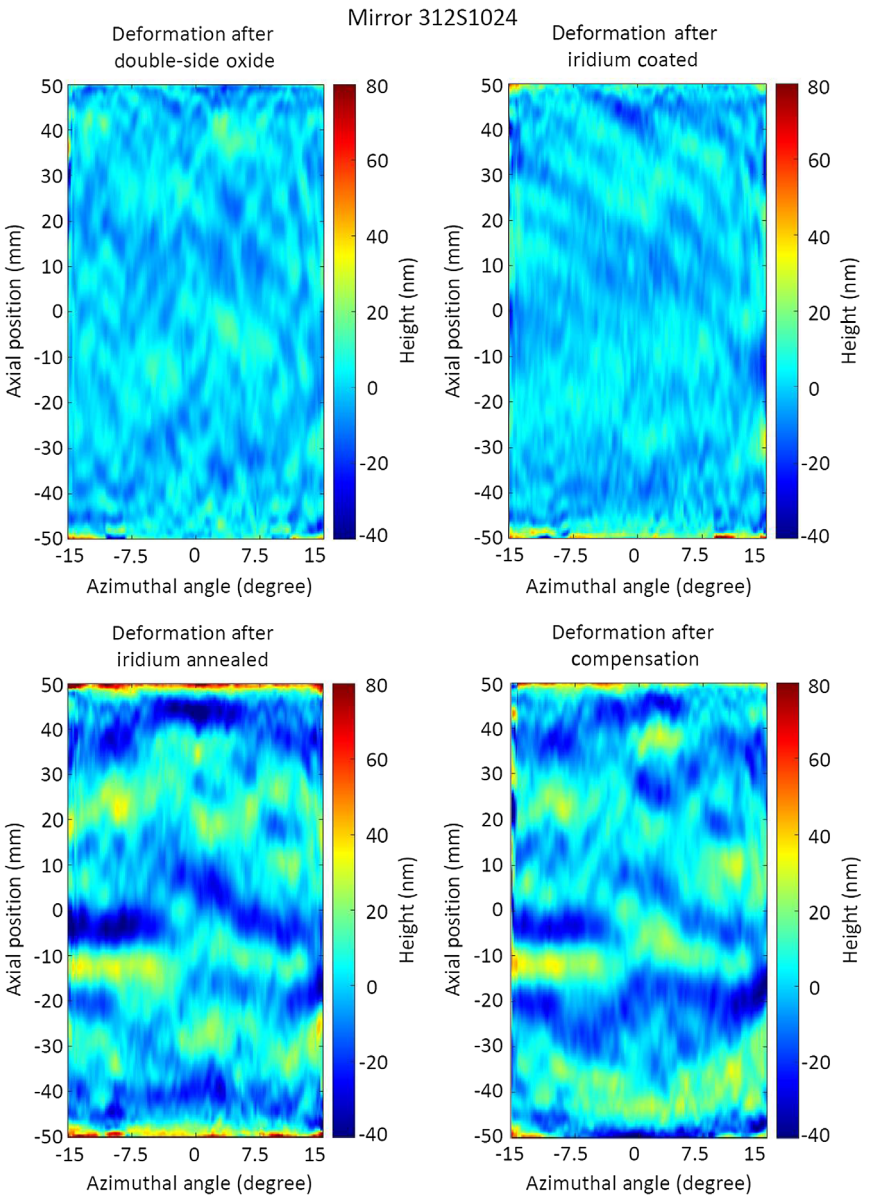


Fig. 10 Measured mirror surface deformations relative to the shape before oxidation (step 0). The plots are Legendre polynomials fitted to the data but excluding zeroth to fourth orders.

Possible explanations for this phenomenon are still under investigation. Multiple solutions will be followed up to eliminate the mid-frequency errors, including improvements of the coating stress uniformity in annealing process and stress calculations with higher-order Legendre polynomials. Progress will be reported in future work.

4 Conclusions

We have developed a thermal oxide patterning method for compensating silicon mirror distortion induced by coating stress. This method has been demonstrated by compensating the coating stresses in 20-nm-thick iridium films on two pieces of GSFC-fabricated silicon mirrors which are 100-mm long, 0.5-mm thick, having 312-mm radius of curvature, and 30 deg in azimuthal span (Wolter-I geometry). As subtasks for this effort, we have developed (1) a process to design the thermal oxide hexagon pattern, (2) an annealing process to stabilize and adjust the coating stress, and (3) a photolithographic process to create hexagon patterns on the back side surface of the mirror, which are curved and rough. Experimental results show that we have successfully reduced the coating-induced distortion by a factor of ~5 in RMS height errors and ~4 in RMS slope errors, which corresponds to the 0.5 arc sec level in RMS slope errors. The residual errors are dominated by mid-frequency stress ripples which appear to be generated by the annealing process.

For future work, we plan to improve the stress compensation precision by eliminating the mid-frequency residual errors. Annealing process parameters will be optimized, and higher-frequency stress functions will be used to design oxide patterns for better compensation.

Acknowledgments

This work was supported by NASA Grant Nos. NNX14AE76G and NNX17AE47G.

References

1. J. A. Gaskin et al., "The Lynx X-ray Observatory: concept study overview and status," *Proc. SPIE* **10699**, 106990N (2018).
2. M. C. Weisskopf, S. L. O'Dell, and L. P. V. Speybroeck, "Advanced x-ray astrophysics facility (AXAF)," *Proc. SPIE* **2805**, 2–7 (1996).
3. W. W. Zhang, "Manufacture of mirror glass substrates for the NuSTAR Mission," *Proc. SPIE* **7437**, 74370N (2009).
4. W. W. Zhang et al., "Astronomical x-ray optics using mono-crystalline silicon: high resolution, light weight, and low cost," *Proc. SPIE* **10699**, 106990O (2018).
5. E. Spiller, *Soft X-ray Optics*, SPIE, Bellingham, Washington (1994).
6. K. Chan et al., "Reflective coating for lightweight x-ray optics," *Proc. SPIE* **8443**, 84433S (2012).
7. D. M. Broadway et al., "Achieving zero stress in iridium, chromium and nickel thin films," *Proc. SPIE* **9510**, 95100E (2015).
8. B. D. Chalifoux et al., "Simulations of film stress effects on mirror segments for the Lynx X-ray Observatory concept," *Proc. SPIE* **5**(2), 021004 (2019).
9. K. Chan et al., "Coating thin mirror segments for lightweight x-ray optics," *Proc. SPIE* **8861**, 88610X (2013).
10. B. Chalifoux et al., "Compensating film stress in silicon substrates for Lynx x-ray telescope mission concept using ion implantation," *Proc. SPIE* **10699**, 1069959 (2018).
11. H. Mori et al., "Reflective coatings for the future x-ray mirror substrates," *Proc. SPIE* **10699**, 1069941 (2018)
12. Y. Yao et al., "Stress manipulated coating for fabricating lightweight x-ray telescope mirrors," *Opt. Express*, **23**(22), 28605–28618 (2015).
13. C. T. DeRoo et al., "Deterministic figure correction of piezoelectrically adjustable slumped glass optics," *J. Astron. Telesc. Instrum. Syst.* **4**(1), 019004 (2018).
14. Y. Yao et al., "Thermal oxide patterning method for compensating coating stress in silicon substrates," *Opt. Express* **27**(2), 1010–1024 (2019).
15. Y. Yao et al., "Thermal oxide patterning method for compensating coating stress in silicon x-ray telescope mirrors," *Proc. SPIE* **10699**, 1069942 (2018).
16. J. P. Lehan et al., "Progress toward a complete metrology set for the International X-ray Observatory (IXO) soft x-ray mirrors," *Proc. SPIE* **7437**, 74370R (2009).

Biographies of the authors are not available.