Collaborative Platform, Tool-Kit, and Physical Models for DfM

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ABSTRACT

Exploratory prototype DfM tools, methodologies and emerging physical process models are described. The examples include new platforms for collaboration on process/device/circuits, visualization and quantification of manufacturing effects at the mask layout level, and advances toward fast-CAD models for lithography, CMP, etch and photomasks. The examples have evolved from research supported over the last several years by DARPA, SRC, Industry and the Sate of California U.C. Discovery Program. DfM tools must enable complexity management with very fast first-cut accurate models across process, device and circuit performance with new modes of collaboration. Collaborations can be promoted by supporting simultaneous views in naturally intuitive parameters for each contributor. An important theme is to shift the view point of the statistical variation in timing and power upstream from gate level CD distributions to a more deterministic set of sources of variations in characterized processes. Many of these nonidealities of manufacturing can be expressed at the mask plane in terms of lateral impact functions to capture effects not included in design rules. Pattern Matching and Perturbation Formulations are shown to be well suited for quantifying these sources of variation.

Keywords: Design for Manufacturability (DfM), optical imaging, linewidth variation, aberrations, masks, CMP, etch, metrology, spillover, pattern matching, timing, signal integrity

1. INTRODUCTION

Semiconductor Manufacturing is facing severe and worsening challenges in achieving yields, delivery schedules, and costs. Major efforts have been spawned within and among IEDM's, Foundries, Fab-Less design companies and EDA vendors to address these issues in what generally fit under the heading of Design for Manufacturability (DfM) and even Manufacturability for Design (MfD). The challenge is to be able to integrate the complexity and enormity of subtle processing effects that impact circuit performance through out the semiconductor manufacturing flow.

The need to consider physical effects during the design process has been recognized for years including this fifth SPIE conference on this topic. The dialog over the last 10 years has migrated from Optical Proximity Correct (OPC) to Process Proximity Corrections (PPC) as more processing effects were considered. The strategy has been to pay attention to the dominant nonidealities in processing. A seminal result from the 2005 SPIE conference by an IBM team [1] was that DfM could be a win for design as well as a win for manufacturing. Example layouts were shown that were smaller in area as well as more acceptable in manufacturing. This indicates that major gains are possible by collaborating across previously ridged boundaries. It may well be that designers are as good at dealing with integrating complexity as process technologists and Technology CAD developers. Today the strategy is to consider physical effects in the context of the full chip design and to begin to do so early in the design flow at high levels of abstraction with commensurate fast but approximate physical models [2].

This paper looks at the emergence of new DfM strategies based on the experience of the authors in university research on characterization, physical modeling and control. The paper begins with an overview of the requirements for DfM approaches and the leverage that the authors bring from ongoing process-centric collaborative research. Specific projects

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with DfM and potential DfM content are then described starting from collaborative platforms. Approximate physical models based on spillback functions and convolutions are introduced and their applications to device variation in layouts and interactions between standard cells are then considered. Relevant results in modeling CMP, etching and assigning causes to statistical variation are then overviewed. Applications to estimate variations interconnect and signal delays and integrity that combine the above are then discussed. Finally, the role of mask imperfection is briefly explored.

2. DfM REQUIREMENTS

DfM requires accounting for manufacturing variations during early stages of the design flow as influenced by the attributes of the design itself. This leads to Requirements for DfM that differ from requirements for traditional physical modeling and Technology CAD tools. These differences are summarized in Table I. One of the overarching requirements is to integrate the complexity and balancing of trade-offs across all significant contributions to variations. The platforms must thus have broad reach and be flexible to adapt to new circuit performance concerns and sources of variation as they are discovered. It is also important that the platforms promote collaborations among the historically distinct disciplines and facilitate these collaborations using metrics familiar and intuitive to each discipline. New functionalities for managing the integration task must also be provided. The physical models are distinct from those traditionally used in Technology CAD for process simulation as they must be several orders of magnitude faster and yet at least first-cut accurate. The scope of these models includes every process step and even interactions between process steps. The models must also evolve rapidly as evidenced by constant evolution of the manufacturing technology such as has occurred with resolution enhancement, high-NA and immersion lithography.

Platforms to Integrate Complexity

- **Broad Reach to encompass all contributions to complexity**
- **New Collaborations (Process, Device, Design) supporting the viewpoint of each with the intuitive terminology of each**
- **New Functionalities for Task Management, Visualization and Assessment**

Physical Models

- **Very fast and first-cut accurate**
- **Complete set of processes and their interactions:**
  - **Litho, CMP, Etch, Device, Metrology; Litho-CMP, etc.**

Table 1: Requirements for DfM that differ from those for traditional physical modeling with Technology CAD.

3. LEVERAGE FROM UNIVERSITY RESEARCH

The physical understanding from research on process modeling, characterization and control can provide a physical base and modeling strategies for DfM and MfD. The Semiconductor Research Corporation (SRC) has historically supported process modeling at a number of universities. DARPA has also contributed to investigating emerging lithography techniques and associated cross-cutting resist and modeling capabilities. In addition to developing the physical understanding of process modeling, university research has also provided new tools and concepts that can be leveraged. In the authors' particular case this has included rigorous simulators for aerial images (SPLAT) and electromagnetic scattering (TEMPEST), lateral spillback concepts that characterize aberration effects, fast-CAD software for rapidly convolving local spillback functions throughout a layout, and a collaborative platform for DfM that integrates across process, device and circuit design. SRC is currently supporting further research to create process aware design.

The authors have also had the opportunity to test their ideas in practice through collaboration with approximately 20 companies in the Feature Level Compensation and Control (FLCC) project under the State of California U.C. Discovery Program. The FLCC project includes synergistic work on lithography, etch, CMP, devices and metrology. Industry advice and involvement has allowed us address relevant issues and to conduct experiments in our laboratories, production tooling, emerging tooling and silicon chip processing.

4. COLLABORATIVE PLATFORM FOR DfM AND PROCESS AWARE EDA TOOL-KIT

The authors are exploring prototype software approaches for integrating process complexity in a manner that can be effective in DfM. One concept is that of a “Collaborative Platform for DfM” that has given rise to the title of the current paper [3]. The concept shown in Figure 1 is to provide a Process/Device/Design framework so that process technologists, device technologists and circuit designers can each visualize from their familiar point of view the consequences of process variations on circuit performance. The “big picture” idea of this platform is to shift the statistics in statistical timing and power analysis upstream from gate level CD distributions to a more deterministic set of sources of variations in characterized processes. The platform utilizes a Parametric Yield Simulator to predict circuit variability of a circuit design layout and for a set of characterized sources of variation. For example the aerial image of a layout is simulated across a predefined process window and resulting non-idealities in geometrical features are communicated through to circuit simulators, where circuit robustness and yield can be evaluate in terms of leakage and delay variability. This simulator is able to identify problem areas in a layout and quantify them in terms of delay and leakage in a manner in which designers and process engineers can collaborate together on an optimal solution to the problem. A complementary set of validation and characterization experiments has been designed and is currently being executed at Cypress Semiconductor and now the Silicon Valley Technology Center on a 65nm short loop enhanced-NMOS process flow. The goal of these experiments is to gain further insight into advanced processing technologies and create a unique opportunity for collaborative experiments between groups in different disciplines.

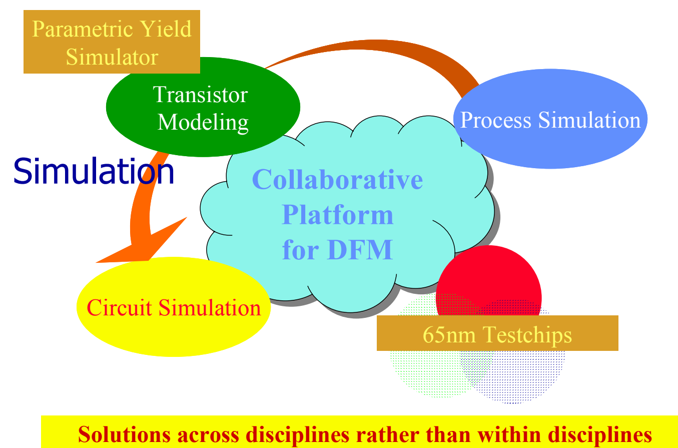

Figure 1: Collaborative Platform for DfM concept showing the interaction between process technologists, device technologists and circuit designers as well as experimental verification.

The Parametric Yield Simulator (PYS) is a comprehensive simulation flow from processing to circuit simulation based on existing EDA tools. In the current version the automated flow from GDSII to HSPICE circuit analysis is implemented using Mentor Graphics Calibre Work Bench, HSPICE, and a set of Perl and TCL scripts. This flow has been implemented in a modular fashion with distinct breaks between poly gate extraction, transistor model generation, and circuit implementation (Figure 2). The processing module was built based on Calibre Printimage to model the lithography step through a specified process window. The device module builds a BSIM equivalent transistor model that can handle non-rectangular gates. Finally, the third module injects all the calculated transistor lengths into an HSPICE netlist for circuit simulation. The whole flow can be wrapped in Perl scripts for simulating circuits across a process window or with different processing variations.

We are also exploring prototypes of tools to utilize throughout the design flow in a Process Aware EDA Tool-kit. For example, we are exploring robustness metrics for circuit layouts based on parametric yield simulation that allow chip-plan context-specific trade-offs to be made in area and robustness during design. These metrics would be suitable for either automated or hand crafted design. To aid designers in reviewing and addressing design issues we are also exploring the Drag-and-Drop Hot-Spot Fixer shown in Figure 3. Here the design on the left has a hot-spot associated with the feature passing the contact pad. The right side of Figure 3 depicts how estimates of image changes in real-time could be utilized to track the reduction of the initial hot-spot and the accidental creation of two additional hot-spots as the translated feature interacts with the features to the right.

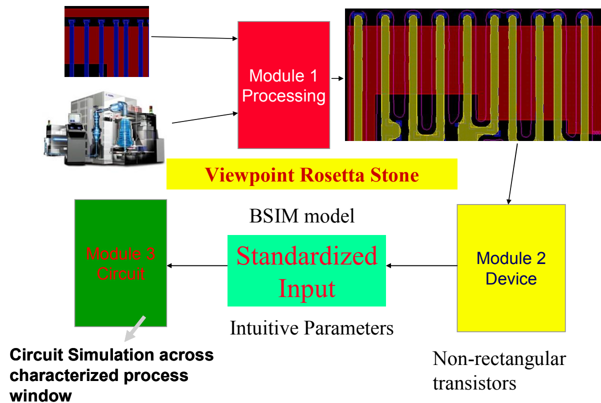

Figure 2: Collaborative Platform for DfM: Implementation showing the use of layout (GDSII), nonrectangular transistor models, BSIM models, and HSPICE as a means of communicating.

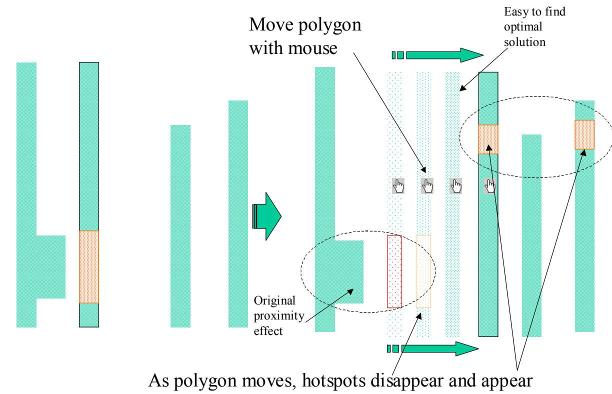

Figure 3: Drag-and-Drop Hot-Spot Fixer that displays real-time to the designer the reduction of an initial hot-spot as it is fixed by moving the layout and the inadvertent creation of other potential hot-spots.

5. SPILLOVER, SPILLBACK AND PATERN MATCHING

The concept of utilizing Maximum Lateral Impact Functions to quickly search layouts for problematic processing issues arose out of consideration of lens aberration effects (including defocus) in optical projection printing [4,5]. It is well know that aberrations spread light from the targeted image point laterally. In fact, the electric field incident on the wafer can be approximated as the diffraction limited electric field plus an additional spillover electric field. As for many physical effects this spillover only depends on the position of the observation point relative to the source point. Figure 4 illustrates how the additional spillover field from a small region of a line end of a transparent rectangle (shown in inverse tone as a dark rectangle) spills electric fields laterally to the elbow shaped transparent feature (also shown in inverse tone). Since every transparent point on the mask spills light laterally in the same manner, each small region on the transparent elbow spills light laterally onto the line end. In general it would be necessary to add up (integrate) these spillover contributions over the adjacent layout to determine the pattern dependent lateral effects. This point-by-point spillover addition can be viewed alternatively as first computing the spillback function for a full field of uniform intensity point sources and then convolving this spillback function with the layout. We term this spillback function the Maximum Lateral Impact Function and consider the integration over the layout Pattern Matching that determines the Match Factor. Finding problematic processing issues is thus reduced to finding locations in a layout where Match Factors with large magnitudes occur.

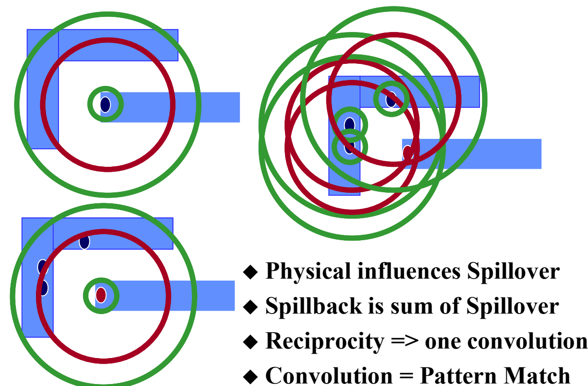

Figure 4: Concept of lateral spillover from a rectangular opening (shown in reverse tone), spillover from multiple sources on an adjacent elbow, and evaluation of the lateral impact by integration of a spillback function over the surrounding layout. The latter can be viewed as computing the degree of similarity of the layout to the spillback function and carried out in graphics like algorithms and hardware.

When applied to optical imaging there are interesting additional considerations due to the fact that, that the image is the time-average of the square of the electric field. One additional consideration is that the relative phase of the illumination on the mask at the source and observation locations must be included. That is the partial coherence of the illumination must be included in computing the spillback. Examples of the mutual coherence function are available for top-hat, annular, quadrapole and dipole illumination [6]. A second additional consideration arising from the time-average square of the fields is that image by itself cannot be calculated from a single Match Factor. Instead, however, where effects are small a perturbation ΔI of the original image can be computed. The edge placement error EPE or ΔE can then be estimated by dividing ΔI by the slope of the original image. This has worked very well for computing defect interactions with features [7].

For aberrations it is interesting that the spillover is real for odd aberrations like coma and trefoil and imaginary for even aberrations such as focus, spherical, and astigmatism [4]. Weak points such as line ends are thus subject to linear change with increasing coma and quadratic change with increasing defocus. This is illustrated in Figure 5 for the case of two opaque lines circulating around the line end of a third opaque line.

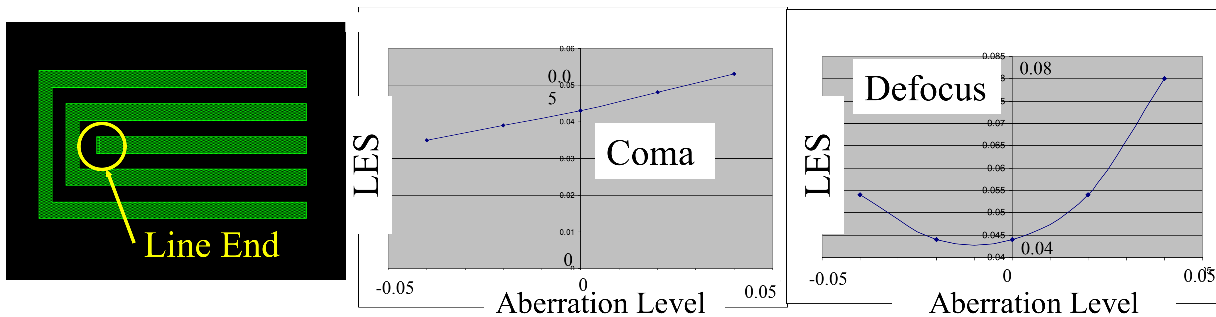

Figure 5: Line End Shortening (LES) for the layout insert as a function of aberration level for coma (linear) and defocus (parabolic).

The spillback match factors are even larger for phase-shifting masks. This is because the dark chrome regions are replaced by a region that transmits electric fields that are of opposite phase and drive the negative lobes that typically are present in the Maximum Lateral Impact Function. For a 6.25% attenuating phase-shifting mask (ATT-PSM) the transmitted electric field is 25% of the electric field of the clear area. For an alternating phase-shifting mask (ALT-PSM) the transmitted electric field is 100% of the electric field of the clear area. For the example line-end and surround in Figure 5 this increases the MF for the line as follows. For coma it is 0.075 for binary, grows by 25% to 0.094 for ATT-PSM and doubles to 0.15 for ALT-PSM. The Match Factors for focus for the three cases are 0.309, 0.318 and 0.342 and show proportional growth. The line end image slope increases from 6.95, to 7.93 and finally to 9.1 μm^{-1} with the use of ATT-PSM and ALT-PSM. This partially but not completely mitigates the increase in spillback.

Maximum Lateral Impact Functions have been developed for a variety of optical processing effects. These include lack of uniformity in quadrapole and dipole illumination, high-NA vector effects, phase-etch errors in fabricating phase-shifting masks and the degree of polarization in the illumination [8,9]. These Maximum Lateral Impact Functions can also be used to develop of phenomena specific test patterns. An example is the generation of Design-Rule compatible monitors by the automatic morphing of the focus ring structure into acceptable layouts by J. Holwill in this Proceeding [10].

6. PATTERN MATCHING FAST-CAD FOR LITHOGRAPHY

We are exploring the use of pattern matching to develop fast-CAD tools for making litho aware EDA tools. This matching process was implemented in a sophisticated algorithm and code termed the Pattern Matcher by Frank Gennari [11]. It is orders of magnitude faster than OPC for first-cut estimates. This code read in a full chip 5.6GB hierarchical GDSII layout with OPC that contained over a hundred million rectangles and polygons files and perform matches on corners of all features for a single pattern on a 128 x 128 grid in 17 minutes using 1.3 GBytes memory on a 2.8 GHz desktop. One application of Pattern Matching is in examining aberration induced layout dependent effects. To calibrate

such tools we begin by examining effects on simple patterns such as was shown above in Figure 5. We then move on to automating the process on somewhat larger hand-drawn layouts. This consists of keep a variety Match Factor locations and exporting the layout and cut-line to a process simulation for aerial image evaluation. The change in intensity in simulation with and without the aberration present is then plotted versus the corresponding Match Factor. Figure 6 shows an instance of a match for coma and the resulting correlation plot for a small layout of test structures. Note that the Match Factors are both negative and positive and that the intensity change is also both negative and positive. The overall trend is that the intensity change is about 20% of the clear field intensity and that multiplying the Match Factor for a give shape by 0.5 is a good first order estimate of the intensity change.

Pattern Matching is useful for screening of unwanted interactions among standard cells. Many combinations of possible neighbors must be evaluated quickly for a multitude of process window conditions and additional process nonidealities. Figure 7 shows how Pattern Matches can reach from one standard cell to another to pick up the lateral influence between cells. By automating this evaluations process cells that are aggressive neighbors or weak victims can be identified and redesigned.

A major advantage of the Pattern Matching approach is that the Maximal Lateral Impact Functions can capture effects where it is not practical to generate design rules. Specifically as shown in Figure 8 the contributions of next-next neighbors are easily captured without having a geometrical increase in the already hundreds of design rules. Also, as process issues are identified or mitigated, the impact on designs can be re-evaluated through Maximal Lateral Impact Functions in an advisory capacity for the same design rules. The maximum Lateral Impact Functions are also useful in recognizing from wafer measurements those portions of statistical variation that are inherently associated with a small set of process variation causes.

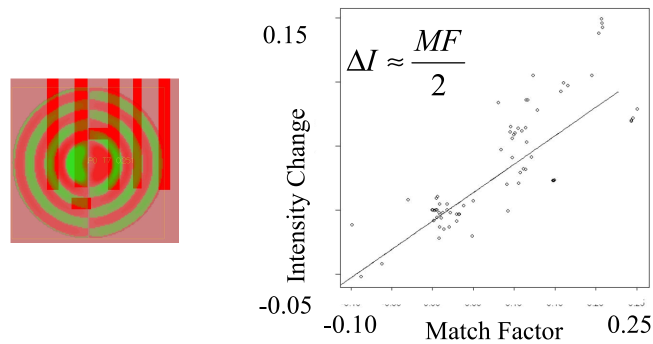

Figure 6: Automatically generated correlation plot for the change on the Line Edge Intensity (LEI) due to 0.025 waves of coma from aerial image simulation versus the Match Factor (MF) for many locations on a hand drawn layout.

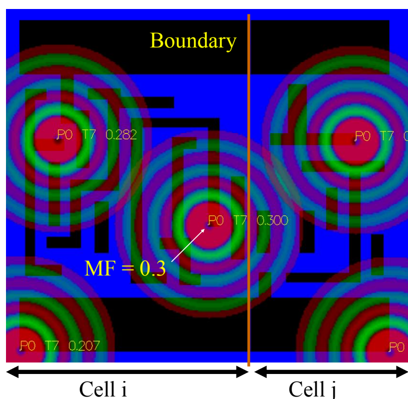

Figure 7: The Pattern Matching from a victim Standard Cell on the left reaches over to include influences from an aggressor Standard Cell on the right.

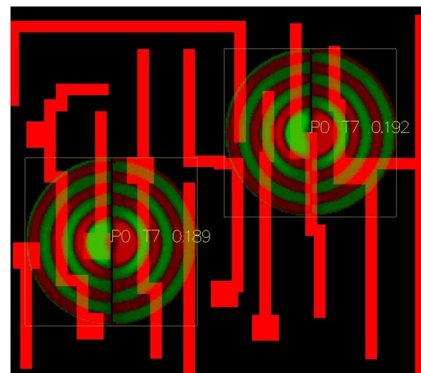

Figure 8: Maximal Lateral Impact Functions for coma captures distant effects where it is not practical to generate design rules for next-next neighbors.

7. MODELING CMP AND ETCHING

The set of assignable causes of circuit variations goes well beyond lithography to other processes. Here ongoing modeling and characterizations studies are expected to play an important role. CMP is an interesting example where models and EDA tools are emerging. A notable new result is a model for CMP that encompasses both the dielectric deposition and the polishing process [12]. The model was developed for oxide polishing in a shallow trench isolation process flow. The feature size dependent deposition of oxide was first characterized to account for feature dependent oxide thickness. Next the length scale and separation of the asperities in the polishing pad were characterized. This information was then included in estimating the down force per unit area sufficient to support the pad as a function of feature density and remaining polishing height. This in turn permitted the generation of a die scale map of the oxide thickness remaining versus polishing time. It is likely that the main elements of this approach could be mapped into Pattern Matching Functions and applied to layout layers to obtain a first-cut accurate estimate of variations in interconnect wiring height and insulator thickness early in the design flow.

Plasma etch is also an interesting example. Systematic measurements and simulation matching were made recently for silicon trench etching as a function of critical parameters such as etch gas mixtures, flux of species, and DC bias [13]. The behavior of this parameter set versus spatial reactor position is now being studied through reactor scale [14] and local plasma simulation [15]. The coupling of this reactor, local fluxes and feature scale information is being pursued for modeling feature shape effects and possible LER trends in etching. It is again likely that very fast and first-cut accurate models could be built from the above more comprehensive model.

8. METROLOGY AND CONTROL

A major focus of metrology is to unbundle variation into assignable causes at the lot, wafer, field, die, functional block, and feature level. Across chip linewidth variation ACLV is usually a sizeable part of the entire CD budget. One example can be found in our collaborative studies [16] with industry to minimize variations over a litho/etch sequence. More surprisingly, a recently a collaborative examined the degree to which linewidth variations correlated locally. Surprisingly, correlations of over 0.5 were observed in the few first few mm from the edge of the field [17]. This of course adds credibility to the idea that much of the device variation is deterministic.

9. INTERCONNECT

It is very challenging to accurately predict interconnect delay. It is even more difficult to accurately predict the variation in the interconnect delay that result from process variations. Yet it is well known that the main causes of variation are associated with the drive transistor and to a lesser extend the load transistor, the capacitance and the resistance. We are attempting to develop fast-CAD methods for estimating delay by adding new functionality for estimating capacitance and resistance variation to the circuit simulation in the Parametric Yield Simulator [18]. Our prototype software follows the circuit wiring through various metallization levels and estimates geometrical and subsequent electrical changes as a function of the limited set of dominate assignable causes in lithography, etch and CMP.

An initial study of lithographic effects on a design from the Berkeley Wireless Research Center is available in this conference Proceeding [18]. This circuit design had some 326,000 nets of which about 500 were considered critical in meeting the required slack time. Our prototype software followed the signal through wiring levels 3 and 4. The Match Factors were evaluated at approximately 1 µm intervals to estimate geometry changes in linewidths along the interconnect. This was then used to estimate the changes in capacitance, resistance and delay. The results indicate that process induced variations can reordering the worst case slack time circuits. Computationally, it appears that through Pattern Matching that it is feasible to assess effects of process specific variations in delay estimates with only moderate increases in computation time.

We are also undertaking fast-CAD prototype development to assess effects of process variations on cross-talk. It is essential to look at the variation and correlation of drive strength and capacitance of aggressor and victim circuits. Initial studies show that for typical linewidth and insulator thickness changes that each produce a 6% change in cross-talk that uncorrelated variations in the gate lengths of aggressor and victim circuit drivers can result in a 50% change in the cross-

talk voltage contribution. Correlation of gate variations helps mitigate this cross-talk increase and is thus an important component in first-cut accurate modeling.

10. MASK ISSUES

Mask edge topography and opening aspect ratios are becoming a major challenge for manufacturing with DUV lithography. The chrome thickness of 80 nm is already a concern. In ATT-PSM which is very popular film stacks are noticeably higher and the attenuating layer height to width aspect ratio is approaching unity. Unfortunately the electromagnetic effects at edges contribute effects not accounted for by simple vertical propagation (thin mask) models. The edges impact mask performance and, in fact, it was reported recently that in ordering ALT-PSM masks that the designers are now required to select a single feature size for which the phase-shift will be the desired 180 degrees [19]. We are exploring the severity of these effects, appropriate models for them and a strategy for informing the designers of this additional source of variation. Figure 9, shows the mask geometry and non-vertical movement of the light. The negative and positive values of both the real part and of the imaginary part of the emerging field are then displayed. Finally, the residual bias and unanticipated imaginary part of the emerging field are displayed in the layout for the designer. The lateral spillover of this imaginary contribution with defocus is a concern because it adds an additional linear component to the formerly quadratic behavior of the line edge and line end positions through focus.

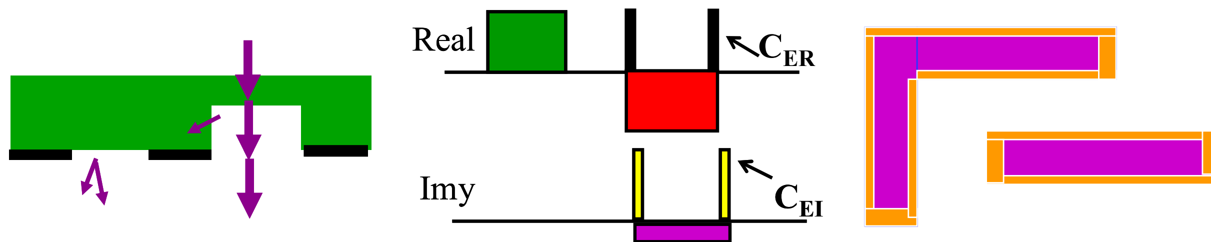

Figure 9: Phase-shifting mask geometry and transverse movement of the light, the positive and negative values of the real part and imaginary parts of the emerging field and the display of the unanticipated imaginary part for the designers.

EUV masks are an even greater challenge due to their use in reflection with off-axis configurations and with the potential for buried nonplanar defects. Ray tracing electromagnetic analysis tools have been developed for rapidly assessing defects and defect-feature interactions [20, 21]. The knowledge base created with these simulators may some day be included in Maximal Lateral Impact Functions for fast-CAD methods of layout vulnerability assessment.

11. CONCLUSION

To be effective DfM must to integrate complexity across disciplines with very fast first-cut accurate models. Information suitable for building fast and first-cut accurate models and feature correlation is available from university research on modeling, experiment and characterization. An important strategy is to shift the statistics in statistical timing and power analysis upstream from gate level CD distributions to a more deterministic set of sources of variations in characterized processes. Many of these nonidealities in manufacturing can be moved to the mask plane and visualized/quantified early in the design cycle via Pattern Matching. Prototype DfM tools and methodologies were shown for Parametric Yield Simulation involving process, device, and circuits, and visualization and quantification at the mask level

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