An overview of low-frequency noise in advanced CMOS/SOI transistors

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ABSTRACT

In this paper, the Low Frequency Noise (LFN) in Partially and Fully Depleted SOI CMOS technologies is overviewed. Static performances of the devices are first presented, then we address, for different types of architectures, the drain current fluctuations in both linear and saturation regimes. A particular attention is paid to the floating body effect that induces a kink-related excess noise, which superimposes a Lorentzian spectrum on the flicker noise. The behavior of this effect with the frequency and the physical mechanisms explaining this excess noise, are discussed. The control of this noise overshoot by using a body contact or by applying a back gate voltage is also demonstrated. On the other hand, the LFN in DTMOS, in ohmic and saturation regimes, is studied and the impact of the use of a current limiter (clamping transistor) is thoroughly analyzed. Finally, the influence of the oxide thickness thinning on the noise is shown.

Keywords: SOI, low frequency noise, carrier number fluctuations, Kink-related excess noise, DTMOS.

1. INTRODUCTION

Thanks to their structure, the SOI technologies present several intrinsic properties for analog and RF applications. For instance, as it is well established now, these interesting devices allow the reduction of the power consumption at a given operating frequency. Moreover, the high insulating properties of SOI substrates, in particular with the use of high resistivity material, leads to high performance mixed-signal circuits [1-3]. However, in order to use this kind of devices in such applications, low-frequency noise, which can directly impact RF or analog integrated circuits, needs to be thoroughly evaluated. Following the specifications of the ITRS Roadmap, the 1/f-noise amplitude is predicted to decrease in modern technologies. But, the maximum signal is also lowered with decreasing operation voltage leading to a deterioration of the signal to noise ratio. Therefore, accurate characterisation of the noise behavior has to be established.

In this paper, Low-Frequency Noise (LFN) in N- and P-channel SOI MOSFETs is widely investigated. An overview of the LFN behavior for two different architectures, fully- and partially-depleted Si film, will be achieved. Furthermore, the impact on the electrical noise of the shrinking from 2µm down to 0.12µm SOI CMOS technology node will be shown, with three different types of layout: floating body, DTMOS and body-contacted. A particular attention will be paid to the floating body effect that induces a kink-related excess noise, which superimposes a Lorentzian spectrum on the flicker noise. The behavior of this effect with the frequency and the physical mechanisms explaining this excess noise, such as trap-assisted generation-recombination noise or shot noise amplified by floating body effect, will be discussed. The control of this noise overshoot by applying a back gate voltage will also be demonstrated and the impact of the gate oxide thickness shrinking on the noise will be shown.

2. EXPERIMENTAL DETAILS

Partially and Fully depleted SOI CMOS technologies, processed on Unibond substrates, were used in this study. For PD technology, three different types of layout were considered: floating body (FB), body-contacted (BC) and Dynamic-threshold SOI MOS (DT). Front oxide thickness was T_{ox1}= 4.5nm and 2nm for 0.25µm and 0.12µm technology nodes,

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respectively. Silicon film thickness T_{Si}=150 nm for PD devices and 40 nm for FD ones and back oxide thickness T_{ox2}=400 nm. A wide range of channel lengths was considered, from 2 down to 0.12μm. Noise measurements in both linear and saturation regimes were carried out in the 1 Hz to 100 kHz frequency range using a dynamic signal analyser (HP 35665A) and a BTA noise probe.

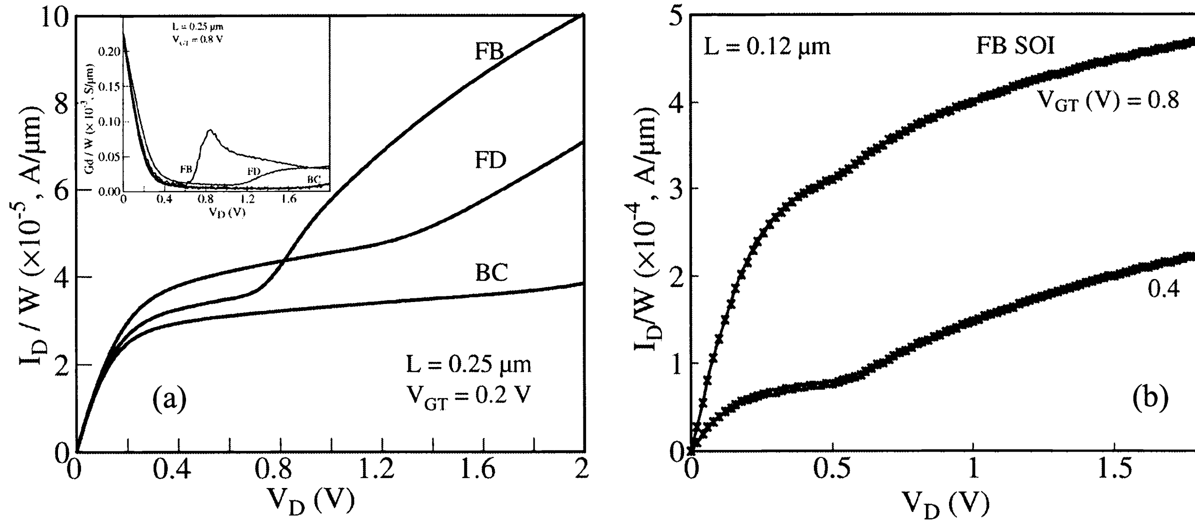

Figure 1 : Output drain current, normalized by the width W, versus drain bias for (a) different layouts with L= 0.25 μm and for (b) FB-PD at two front gate biases with L= 0.12 μm. The inset shows the output conductance for 0.25μm FB-PD, BC and FD SOI devices.

In Figure 1.a are shown, for the various structures, the output drain current characteristics for 0.25 μm channel length. A substantial and moderate Kink effect, associated with a hump of the conductance, as plotted in the inset, are clearly observed in the case of FB-PD and FD devices, respectively, however, it is completely suppressed for body-contacted devices. Figure 1.b represents the output characteristics of a 0.12 μm long transistor under two different front gate biases. The evolution of the Kink effect with V_{G1} is clearly shown.

3. LOW FREQUENCY NOISE in PD and FD DEVICES

We will now consider low frequency noise measurements carried out for PD and FD devices in both linear and saturation regimes to identify the main noise sources as well as the trap densities at the front gate oxide interface.

3.1 Measurements in linear regime

Figure 2 shows, in ohmic operation (V_D=50mV), the normalised drain current power spectral density S_{ID}/I_D^2 plotted as a function of the drain current for N-channel PD-SOI MOSFETs (Fig. 2.a) and for N-channel FD-SOI MOSFETs (Fig. 2.b) for two channel lengths: L=0.25 and 0.12 μm. In this plot, the straight line represents the front gate power spectral density S_{VG} multiplied by the ratio $(G_m/I_D)^2$ where G_m stands for the gate transconductance. A good correlation is obtained between these two amounts, confirming results predicted by the Mc-Whorter model which associates the 1/f noise to carrier number fluctuations [4].
In this model, the fluctuations of the drain current are due to those of the inversion charge near the silicon-silicon dioxide interface caused by the dynamic trapping and detrapping of free carriers into traps located in the oxide near the interface. The normalized drain current spectral density is given by [5] :

$$\frac{S_{ID}}{I_D^2} = \left(\frac{G_m}{I_D}\right)^2 S_{VG} \tag{1}$$

where G_m is the gate transconductance and S_{VG} is the equivalent input gate voltage spectral density.

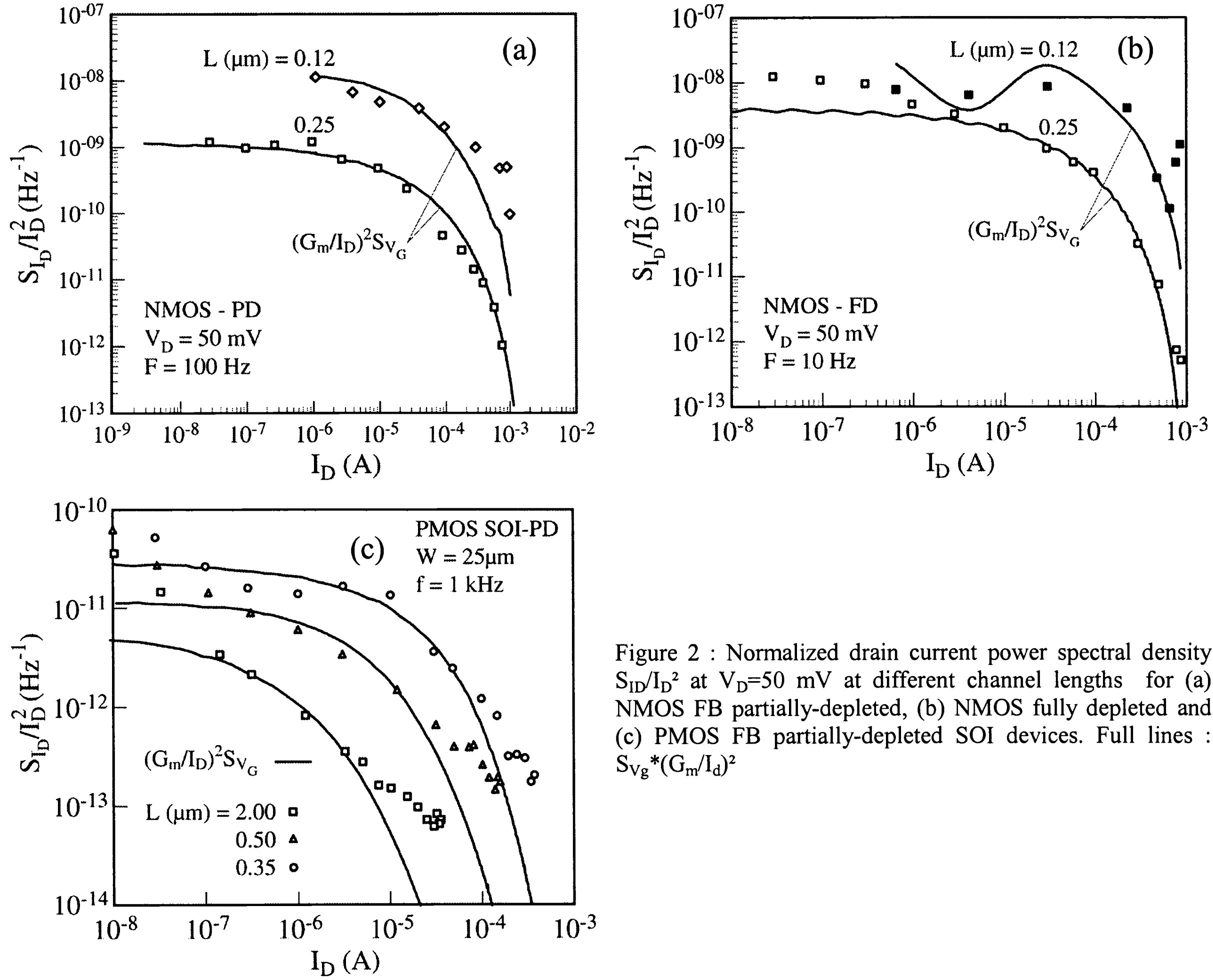

Figure 2 : Normalized drain current power spectral density S_{ID}/I_D^2 at V_D=50 mV at different channel lengths for (a) NMOS FB partially-depleted, (b) NMOS fully depleted and (c) PMOS FB partially-depleted SOI devices. Full lines : $S_{Vg}*(G_m/I_d)^2$

Moreover, some difference in strong inversion can be observed (case of P-channel) (Fig. 2.c) which is attributed to the correlated mobility fluctuations. Indeed, by taking into account the dependence of the carrier mobility on the insulator charge (Coulomb scattering), the fluctuations of the insulator charge give rise to a supplementary change of the mobility, which induces an extra drain current fluctuation. The drain current fluctuations can then be evaluated as:

$$\frac{S_{ID}}{I_D^2} = \left(1 \pm \alpha \mu_{eff} \, Cox \frac{I_D}{Gm}\right)^2 \frac{Gm^2}{I_D^2} S_{VG} \quad (2)$$

where μ_{eff} is the effective mobility, C_{ox} is the gate oxide capacitance and α is a parameter of the order of 10^4 V/s.

Using the following formula given by Christensson [6], it is then possible to evaluate the trap density at the front gate oxide, which is a good indicator of the noise magnitude: $S_{VG} = \frac{\lambda q^2 kT N_t}{W L C_{ox}^2 f}$, where λ stands for the tunneling constant (λ=0.1 nm), N_t is the interface trap density (traps /cm^3/eV), and f the frequency (Hz).

For PD devices, N_t values between 2 to 7.10^{17}/cm^3/eV were calculated, showing a moderate increase when reducing channel length. A similar enhancement of the trap density was also mentioned in a recent paper with small geometry and thin gate oxide on conventional bulk N-MOSFETs [7]. Regarding FD devices, for transistors with a channel length

between 1 and 0.12 μm, we obtained a trap density of about a few 10^{18} /eV/cm^3. This large value may be explained by the influence of the back interface.

3.2 Measurements in saturation mode

Low frequency noise characterization of SOI devices also needs to be carried out in the saturation mode whose bias conditions give birth to the Kink-related excess noise observed in SOI devices. The drain current spectral density S_{ID}, normalised by the width, is plotted (Fig. 3) versus the applied drain voltage V_D for 0.12 μm FB-PD SOI and for L=0.25 μm with FB-PD and Body-Contacted (BC) technologies.

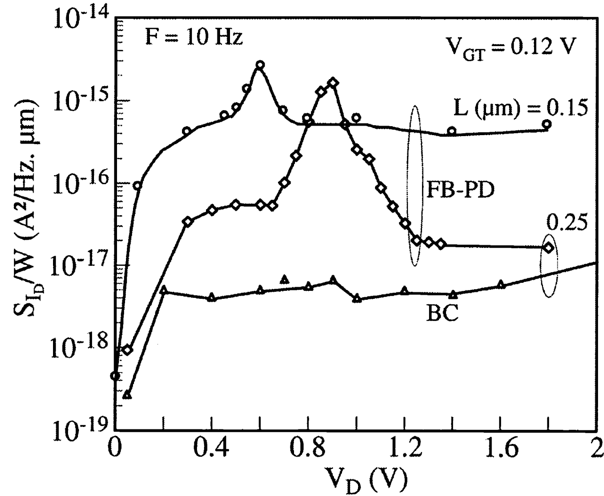

Figure 3: Drain current power spectral density, normalized by the width W, at f=10 Hz for FB-PD devices with two channel lengths (L=0.25 and 0.12μm) and for BC devices with L=0.25μm.

A substantial kink effect is clearly observed in the case of FB-PD devices, and for a drain bias corresponding to the kink effect in static measurements a low-frequency excess noise occurs (Fig. 1). This noise peak shifts with frequency, towards higher V_D. However, the kink effect disappears when the SOI film is contacted to ground. The floating body effect induces a kink-related excess noise, which superimposes a Lorentzian spectrum on the flicker noise, characterized by a corner frequency, fc, and a plateau noise level, S_{ID} (0).

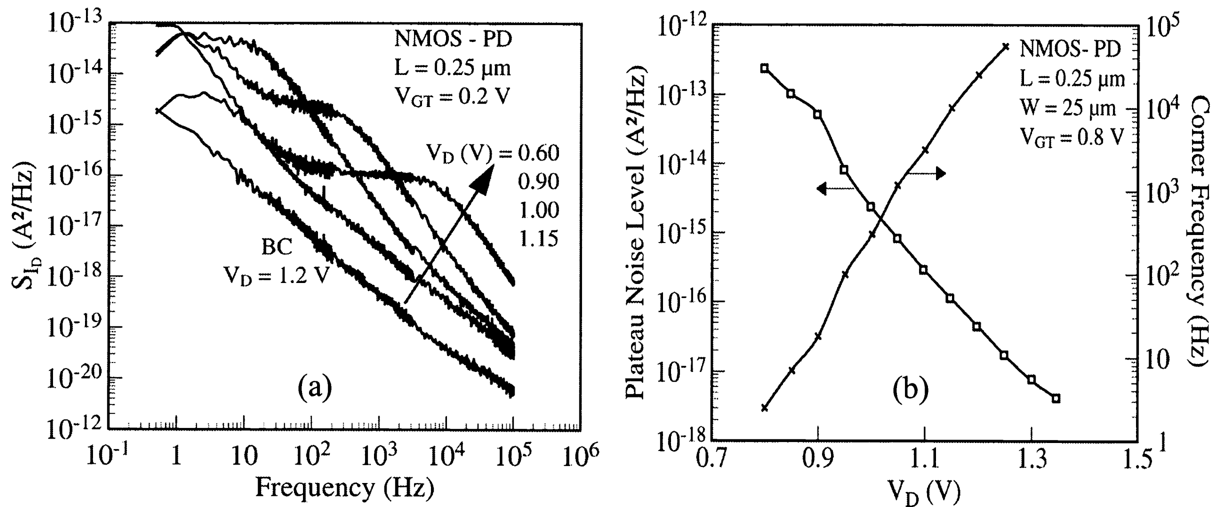

Figure 4: (a) Drain current power spectral density versus frequency for 0.25 μm FB and BC partially-depleted devices, at different drain voltages and (b) Drain bias dependence of the plateau noise level and the corner frequency for 0.25 μm PD device with floating body.

Several mechanisms have been proposed to explain this excess noise, such as trap-assisted generation-recombination noise [8] or shot noise amplified by floating body effect [9]. This behavior is clearly shown in Fig. 4.a for 0.25 μm PD device for different V_D. It is important to note that the corner frequency and the plateau noise level of the Lorentzian spectrum depend both on the drain bias (Fig 4.b).

For PD devices, fc increases and the noise level of the plateau of Lorentzian spectrum decreases continuously as the drain bias is enhanced. This is due to a close correlation between the substrate current, I_B, and the kink phenomenon. The noise plateau level is reversely proportional to I_B and the corner frequency is proportional to the substrate current. Moreover, a relevant point here is the difference between the kink noise overshoot for 0.25 and 0.12μm PD technologies. The magnitude for L=0.12μm is only one decade high, contrary to the 0.25 μm SOI CMOS technology for which two orders of magnitude were obtained.
The drain current noise spectral density has also been measured versus V_D for 0.25μm N-channel FD-SOI at different back-gate voltages (Fig. 5). A moderate kink effect has been observed at V_{G2}=0V in static measurements (Fig. 1.a). As a consequence, the excess noise is almost suppressed at V_{G2}=0V and f=10Hz (Fig. 5.a). When negative back-gate bias is applied, the dc-kink is accentuated and therefore the excess noise is enhanced. This is due to the transition from moderate full depletion to partial depletion regimes. However, at higher frequency (f=100 kHz) and V_{G2}=0V, a notable noise overshoot is obtained (Fig. 5.b). Indeed, contrary to very low frequency where *1/f* noise is dominant whatever the drain bias is, the Lorentzian-like noise dominates at higher frequency and the plateau depends on V_D. The impact of the back-gate voltage is also highly dependent on the frequency range. At very low frequency, we can note a significant difference between the $S_{ID}(V_D)$ at V_{G2}=-10V and -15V. In contrast, the same noise level is obtained at f=100kHz for these two different negative back-gate biases.

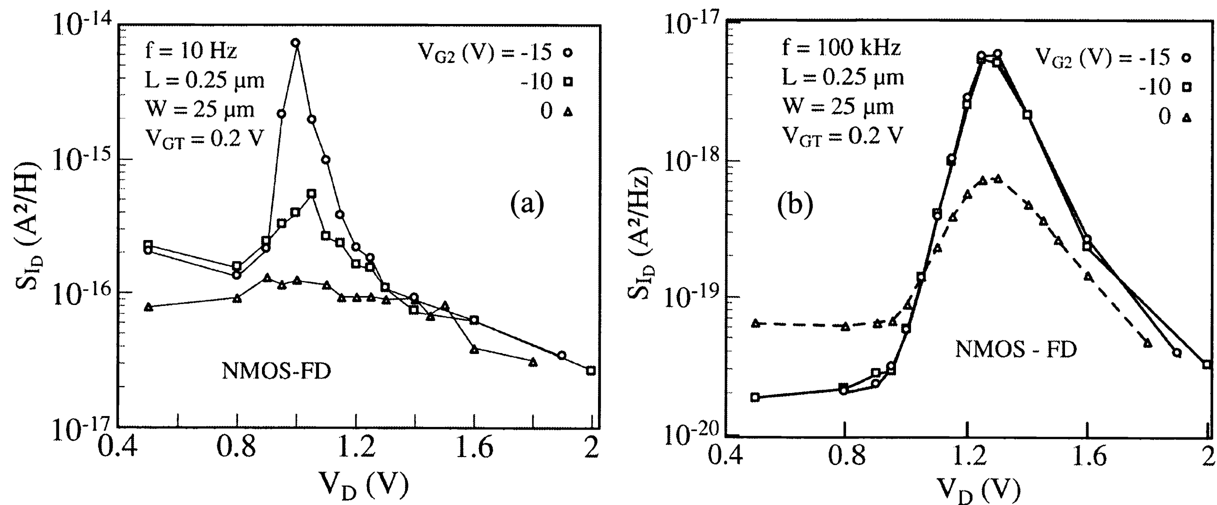

Figure 5: Drain current power spectral density versus drain bias at f= 10 Hz (a) and 100 kHz (b) for FD devices at different back gate voltages. W/L=25/0.25.

4. LOW FREQUENCY NOISE in DTMOS

In this section, Low-Frequency Noise (LFN) in N- and P-channel Dynamic-Threshold MOSFET's on Unibond substrate (SOI) is investigated. Two different types of transistors have been used: with and without current limiter. The LFN in DTMOS is analyzed in ohmic and saturation regimes. The impact of the use of a current limiter (clamping transistor) is shown. An explanation based on floating body effect inducing excess noise is proposed.
Due to the high-leakage current when the body is strongly forward biased, a small size current limiter is added between gate and body in DTMOS structure. Figure 6 shows the two device types. Note that the clamping transistor complicates the design but it prevents the body potential (V_{BS}) to exceed 0.65V and allows operating at 1V gate bias without high gate current. Figure 7 shows drain and gate static currents versus gate voltage for 0.25 μm N-DTMOS with and without clamping transistor. We can note the gate current limitation thanks to the clamping transistor.

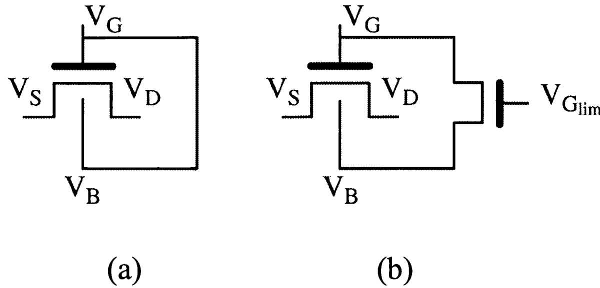

Figure 6: Scheme of the two types of transistors. DTMOS (a) without clamping transistor and (b) with a clamping transistor.

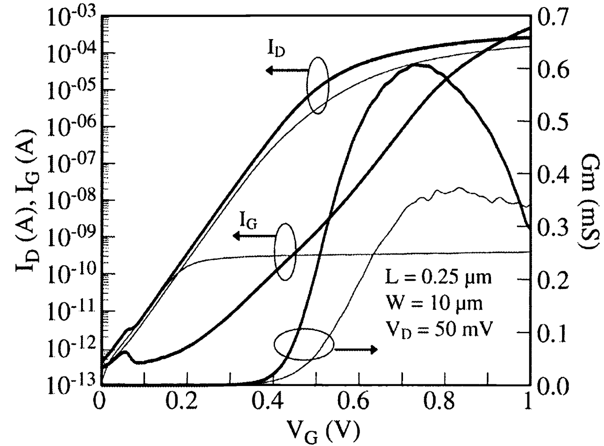

Figure 7: drain and gate currents, and gate transconductance versus gate voltage at V_D=50 mV for 0.25µm DTMOS without and with current limiter.

In Figure 8.a, the drain current power spectral density (S_{ID}) versus frequency is plotted in ohmic region (V_D=50 mV), at various drain current, for 0.25 µm N-channel DTMOS without clamping transistor. 1/f spectrums are obtained, whatever the drain current is. Similar results have also been found for PMOS transistors.

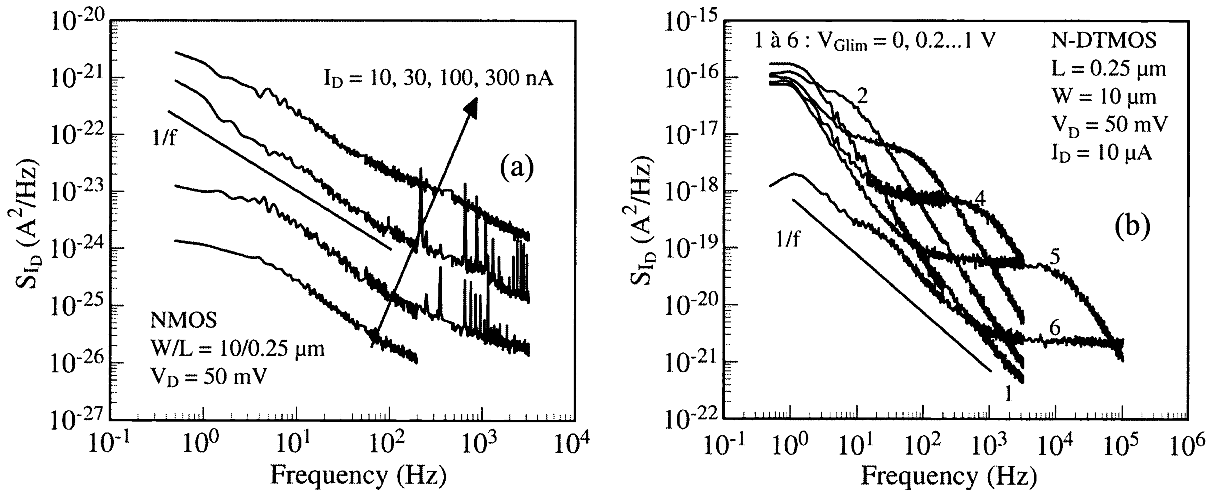

Figure 8: Drain current power spectral density versus frequency in ohmic region for 0.25µm N-channel DTMOS without (a) and with (b) limiter current

However, for DTMOS with a clamping transistor, S_{ID} (f) shows Lorentzian spectrums (Fig. 8.b), which are strongly dependent on the gate voltage of the current limiter (V_{Glim}). The plateau level of the Lorentzian spectrum decreases and the corner frequency increases when V_{Glim} increases (Fig. 8.b).

This behavior is quite similar to the noise overshoot (at high V_D) induced by the kink effect in partially depleted SOI, which is due to the impact ionization mechanism. In our case, V_D is too weak to induce an impact ionization current, however, the clamping transistor current flows through the body inducing an excess noise presenting Lorentzian spectrums. When V_{Glim} is between zero and 1V, the body potential is fixed by the clamping transistor current and, consequently, this current increases the body potential inducing a direct biasing of the source-body junction and a kink-

excess noise like is obtained, even at low drain voltage. At V_{Glim}=1V, the clamping transistor is ON, therefore, the body is directly connected to the gate. In this case, a quasi 1/f behavior is obtained (Fig. 8.b).
Using McWhorter model [4], the noise measurements lead to the determination of the equivalent input gate voltage spectral density, S_{VG} and consequently the trap density N_t. However, in the case of DTMOS the classical determination of S_{VG} and N_t is no longer valid because it considers that the body voltage is grounded. A new formulation of the McWhorter model is then necessary for this kind of devices [10]:

$$S_{I_D} = G_m^2 S_{V_{fb}} \left(\frac{1}{\beta} \pm \alpha \mu_0 C_{ox} \frac{I_D}{G_m} \right)^2 \quad (3)$$

$\beta=1+C_d/C_{ox}$ corresponds to the DTMOS enhancement factor. This factor also explains the higher transconductance for DTMOS than that body-tied one ($G_m(DT)= \beta G_m(BT)$). As a consequence, the drain current noise, S_{ID}, remains the same for the two operation modes.

If now, we take into account the possible correlated mobility fluctuations, the new formulas can be obtained as:

$$S_{ID}(f) = G_m^2 \left(1 \pm \alpha \mu C_{ox} \frac{ID}{G_m} \right)^2 S_{Vfb}(f) \qquad \text{for BT MOSFET} \quad (4)$$

and

$$S_{ID}(f) = G_m^2 \left(\frac{1}{\beta} \pm \alpha \mu C_{ox} \frac{I_D}{G_m} \right)^2 S_{Vfb}(f) \qquad \text{for DT-MOSFET} \quad (5)$$

Noise measurements in the linear region (V_D= 50 mV) have been performed for N and P-channel in BC and DTMOS modes. Using the same transistor for the two operation modes, we can assume that the flat band voltage noise S_{Vfb}, depending on the technological parameters as the trap density N_t, the gate surface and the oxide thickness, is the same for each mode. Taking into account that, for DTMOS, the transconductance enhancement is also due to β, we must finally have no change for the normalized drain current noise between BC and DTMOS.

Figures 9 show the normalized drain current noise versus drain current for N- and P-MOS transistors in each operation mode. A good correlation with $(G_m/I_D)^2$ for N and P channel is obtained and, therefore, it confirms that the noise source in these devices is due to the carrier number fluctuations. Moreover, for all devices, the same drain current noise is obtained, at least in weak inversion. Some difference in strong inversion can be observed (case of 1 μm P-channel BT-MOSFET) which is attributed to the correlated mobility fluctuations.

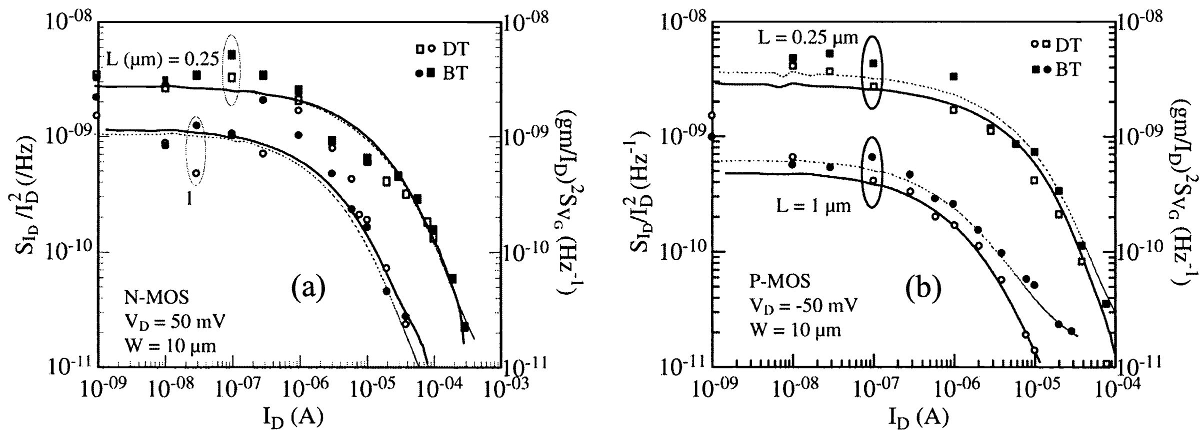

Figure 9 : Normalized drain current power spectral density S_{ID}/I_D^2 at V_D=50 mV and two channel lengths for (a) NMOS and (b) PMOS SOI devices. Full marks for Body-contacted and open marks for DTMOS.

5. GATE INDUCED FLOATING BODY EFFECTS

Low frequency excess noise associated to gate-induced floating body effect is reported in Partially Depleted SOI MOSFETs with ultra-thin gate oxide. This is investigated with respect to floating body devices biased in linear regime. Due to a body charging from the gate, a lorentzian-like noise component superimposes to the conventional 1/f noise spectrum. This excess noise exhibits the same behaviour as the Kink-related excess noise previously observed in Partially Depleted devices in saturation regime. Indeed, scaling metal-oxide-semiconductor (MOS) devices to very-deep submicron dimensions has resulted in an aggressive shrinking of the gate oxide thickness. In this ultra-thin gate oxide range, direct tunneling from the gate clearly appears, and increases exponentially with decreasing oxide thickness. Taking into consideration the case of floating body PD SOI MOSFETs with a 2 nm front gate oxide, the gate-to-body tunneling component becomes large enough to charge the body of the devices, resulting in Gate Induced Floating Body Effects (GIFBE) observed even in linear regime.

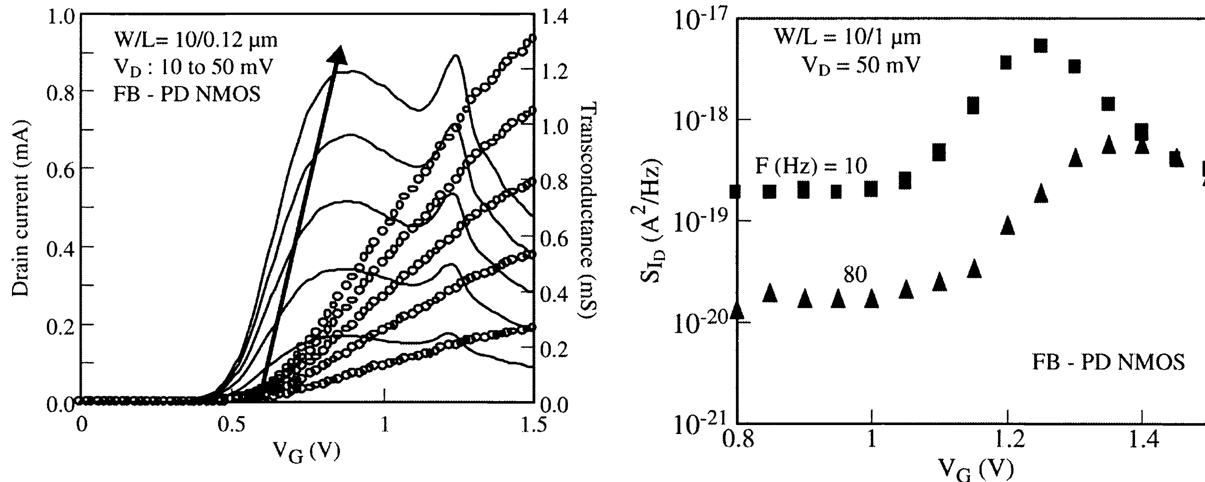

Figure 10: (a) Transfer characteristics I_D and $G_m(V_G)$ of a W/L=10/0.12 μm PD N-MOSFET at low drain voltage (V_d=10 to 50 mV) and (b) Drain current power spectral density of a W/L=10/1 μm PD N-MOSFET with V_d=50 mV. The two different frequencies are f=10 Hz and f=80 Hz.

Figure 10.a illustrates the drain current and transconductance measured in linear regime for V_D= 10 up to 50 mV for a W/L=10/0.12 μm PD N-MOSFET. A sudden increase of the drain current is noticeable close to V_G=1.1-1.2 V whatever the drain bias is, and this results in an unforeseen second hump in the transconductance characteristic, whose value exceeds the normal peak. The same feature is observed for P-MOSFETs. Then, we considered the drain current power spectral density versus the applied front gate bias for two different frequencies (f=10 and 80 Hz). The results are plotted in Figure 10.b for a W/L=10/1 μm FB-PD SOI MOSFET biased with a drain voltage V_D=50 mV. The noise overshoot magnitude attributed to the GIFBE is almost two decades for this device. The shift of the noise peak towards higher gate biases with increasing the measurement frequency is clearly shown in Fig. 10.b.

6. CONCLUSION

An overview of the low frequency noise in both Partially and Fully Depleted SOI CMOS technologies has been given. An enhancement of the overall noise level is noticeable when reducing the channel length. In linear regime, the noise source was attributed to carrier number fluctuations. As regards Partially Depleted devices, the Kink-related excess noise magnitude is reduced with channel length, especially in terms of lorentzian-like spectra and corner frequency evolution. For Fully Depleted devices, a small Kink-effect is observed at high frequency despite a thin Silicon film thickness. The LFN in DTMOS, in ohmic and saturation regimes, was studied and the impact of the use of a current limiter was thoroughly analyzed. Finally, the impact of the oxide thickness thinning on the noise was also shown.

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