Online Training in the Design-Fabricate-Test of Silicon Photonic Circuits

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Abstract: This paper describes the rationale for developing the online course, "Phot1x: Silicon Photonics Design, Fabrication and Data Analysis", offered via edX UBCx, and shares some of our experiences in teaching this course. The course was developed in 2015, and has been offered several times annually to a global audience since then. © 2021 The Author(s)

1. Course overview

1.1. *Motivation for developing the course*

Since 2017, we have been successfully using design-fabricate-test cycles as an experiential learning methodology in integrated photonics, within the SiEPIC program [1]. Design activities motivate students to learn the material much more than conventional lecture-based courses, owing to the requirement that the student designs need to function as expected in order to succeed in the course. In the SiEPIC program, we found that teaching design leads to research, which leads to publications and product development. It also leads to job opportunities and practical experience for students.

Based on our experiences with the in-person workshops offered in the SiEPIC program, we wanted to develop an online course that is accessible to a larger and broader range of audiences (international, different educational backgrounds). The goal was to develop a course that provides students (especially those graduating with an electronics background and working in companies that require a background in photonics) with sufficient experience to get started with designing and analyzing silicon photonic circuits and other fundamental building blocks.

1.2. *Course overview*

Course Learning Objective: This course teaches participants to complete a silicon photonics design-fabricate-test cycle, using a passive silicon photonic process.

Course Philosophy: This course features a highly-compressed design cycle (target 7 weeks) with only 4 weeks for learning how to model photonic components and photonic circuits, and to design a layout which is to be submitted for fabrication, and a target of 3 weeks for fabrication and test. The philosophy is that a participant should be introduced to the complete design-fabricate-test cycle first, and as quickly as possible. Once familiar with the tools, techniques, challenges, limitations, and opportunities, the participant will be in a much stronger position to dedicate more time for a complex design, and better estimate the resources required to complete a silicon photonics design project.

1.3. *Developing the course*

In order to achieve the goal of having a rapid design-fabricate-test cycle, several challenges had to be overcome: 1) having access to an extremely rapid (weeks as opposed to months) and dependable fabrication process, 2) having rapid automated testing, and 3) identifying a simple-enough yet meaningful project that can be designed in a short time. Additionally, our aim was to develop a course that was accessible to a global and diverse audience.

Fabrication was the first challenge. A typical CMOS foundry silicon photonics fabrication process can take many months to complete, and the costs are significant enough to preclude participation by a global audience. Fortunately, basic silicon photonics processes had been developed at several universities using electron beam lithography, and our experience with the process at the University of Washington convinced us that it was mature and reliable enough to contemplate relying on it for courses [2]. With our expectation for rapid turn-around prototyping, the course did face the risk of the fabrication process being unavailable due to a tool being down,

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and universities do not have the luxury of having redundant tools. Fortunately, Applied Nanotools Inc. began offering a commercial silicon photonics process, and we began fabricating with both foundries to mitigate this risk. We aggregate all the students into a Multi-Project Wafer (MPW) where a single chip with a die size of approx 1x1 cm is fabricated. Each participant is given an area of 605 μm x 410 μm, sufficient to fit approximately 10 small circuits. This space allocation allows up to 266 designs on the die, hence up to 266 students per class. If space is available, we also allow students to submit multiple designs.

Testing: We built an automated probe station (described in [3], with similar ones commercially available from Maple Leaf Photonics LLC) which consists of the following: 1. desktop computer, 2. fast tunable and sweepable laser, 3. four photodetectors, 4. a surface coupling fiber array, 5. polarization maintaining fibers, 6. a 90 degree polarization rotator fiber, and 7. an automated electronically-controlled moving stage. The instruments were controlled using custom-written Python code on the computer. The code facilitates the communication between the instruments, and performs fine alignment of the fiber array to the devices of interest; this enables the measurement of thousands of devices with optimum light coupling between the fiber array and the silicon photonic chip. The devices students submit for testing are designed to be tested with either quasi TE or TM modes. The coordinates of all the devices are loaded into the software and the automated testing starts. A polarization rotator is added between the laser and the fiber array to launch the TM mode in the chip waveguides. A live video demonstration of the measurement is shared with the students, who can watch a live video of their devices while being measured, captured using an optical microscope, as well as the graphical user interface of the software indicating the parameters used to control the automated stage, giving them a virtual lab experience.

Course project: For first-time designers, an interferometer serves as an excellent project since they are widely used in many applications such as communications (modulation, switching), sensing, and computing (optical, quantum). The circuit students can design is a Mach-Zehnder Interferometer, consisting of grating couplers, two splitters, and optical waveguides. This project allows designers to extract device parameters from their test data, such as waveguide group index, and see manufacturing variability by submitting several design variations. The activities for this project are thus:

1. Model the optical waveguide using a mode solver, and simulate several optical components.
2. Learn the operating principles of the interferometer, and model the photonic circuit using compact models.
3. Design the photonic circuit. Identify design parameter variations.
4. Create and submit a layout for fabrication, including following the fabrication design rules, automated testing constraints, and design submission details.
5. Conduct a design review of three other peoples' designs, and receive feedback.
6. Receive measurement data from fabricated devices. Analyze the data to extract parameters from the measurements and compare them with models. Report on your design results.

For advanced designers, this course is an opportunity to design many other passive devices, such as directional couplers and other splitters; ring, racetrack and disk resonators; Bragg gratings, including grating assisted contra-directional couplers; photonic crystals; multi-mode interference (MMI) couplers; arrayed waveguide gratings (AWG); polarization diversity components; mode-division multiplexing (MDM) components and circuits, and novel waveguides such as sub-wavelength grating (SWG) waveguides and slot waveguides.

2. Lessons learned - what works well for online experiential learning

We developed short, pre-recorded videos (target was 3 min, some were up to 10 min), with each video followed by an activity (analytic calculations, numerical modelling). Tutorials were provided in both video format as well as written notes with detailed steps. This approach allowed students to review the material multiple times, and to ask questions specific to the topic discussed in the unit. Breaking up the content into small units made it more manageable for both students and instructors.

Our approach was a combination of synchronous and asynchronous delivery: synchronous in that the cohort progresses through the course with a fixed schedule, with fixed deliverables (especially submission of the design for fabrication), and asynchronous since the videos are provided pre-recorded and on-demand. This combination provides both the flexibility of the asynchronous approach, but ensures that students stay motivated and maintain course progression provided by the synchronous approach.

Student learning and course pace: The course is paced by walking the students through a new topic every week, which consists of several modules each containing several units. The students' knowledge is tested through problems, which are electronically graded providing students with instant feedback.

Course deadlines: There are two deadlines to graded submissions: soft and hard deadlines. Hard deadlines are set for the circuit layout submission, peer-review feedback, and report submission. However, soft deadlines are set for the problems sets, which gives students the time to complete the modules at their own pace.

Discussion forum: The discussion forum is a great place for students to ask questions. Students can access the discussion forum either through a link at the bottom after each problem set, or can use it to ask any other course-related or general question about silicon photonics. This provides an opportunity to students, not only to alleviate their doubts, but also learn from other students' questions.

Live Q&A sessions: these were well appreciated by the students, very lively, and led to discussions beyond the core topics of the course.

The course requires students to use software for modelling and design. Both commercial and open-source options are provided. The course exposes students to advanced commercial tools that are used in industry. In addition, many students appreciate using open source tools; the course motivated the community to improve upon the open source tools, e.g., adding waveguide generation and netlist extraction functionality to KLayout [4].

The course includes a design review. This is accomplished first by using a peer assessment framework (multiple peers provide written feedback on each student's design), then feedback is provided in a Live session by instructors. These review approaches improved student designs by reducing errors. Design reviews with a large cohort helped us identify common design errors, and develop automated verification (Design Rule Check) in an open-source tool [4] to check for functional verification (waveguide connectivity), and design for test verification (correct grating coupler pitch, orientation, test vectors).

Beyond the course, students have been given the opportunity to send designs to be fabricated in subsequent fabrication runs. This is beneficial to students as it motivates them to pursue further research in the field and inspires them to come up with more creative designs that can lead to publications.

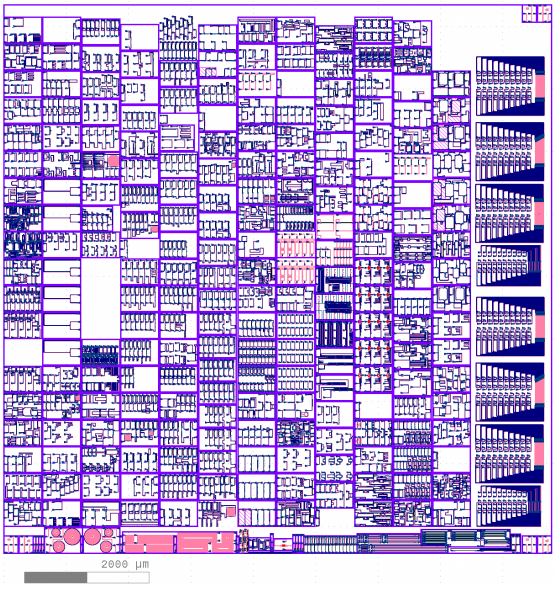

Fig. 1. An example MPW layout for the edX course, showing 233 designs, with a total of 1893 devices.

Table 1. Statistics from the Phot1x edX courses

Cumulative total number of students	1643
Cumulative total number of countries	54
Cumulative total number of course runs	17
Min, Median, Max student age	13, 30, 67
Most popular time of year to start the course	January
Survey respondents: present occupation	N = 609
Graduate Student	35.0%
Industry for an established company	27.4%
Undergraduate Student	7.6%
Researcher at a University	7.1%
Industry for a start-up	6.9%
Post-doc at a University	5.1%
Professor	3.8%
Government	1.6%
Other/unspecified	5.6%

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References:

[1] Silicon Electronic Photonic Integrated Circuits (SiEPIC) program, http://www.siepic.ca/education
[2] Bojko, Richard J., et al. JVST B **29**-6 (2011)
[3] L. Chrostowski, M. Hochberg, "Silicon Photonics Design: From Devices to Systems", Cambridge University Press, 2015
[4] https://github.com/SiEPIC/SiEPIC-Tools