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DEVELOPMENT OF DIGITAL CORRELATED DOUBLE SAMPLING (DCDS) CAMERA ELECTRONICS FOR THE SPACE-BASED WORLD SPACE OBSERVATORY ULTRA-VIOLET SPECTROGRAPH MISSION

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Digital correlated double sampling (DCDS) is an emerging technology for CCD imaging systems in space-based applications. DCDS technology not only provides the low readout noise electronics required by many applications but also offers a range of flexible readout modes that allows the readout noise and pixel frequency to be dynamically adjusted even in operation. This paper describes the DCDS implementation used within the World Space Observatory Ultraviolet (WSO-UV) mission. The latest theoretical and measured noise performance results are presented alongside detailed performance results for the camera electronics including linearity, crosstalk, transient response and gain stability.

STFC RAL Space has developed the DCDS implementation for WSO-UV as part of the camera electronics boxes (CEBs) which house the CCD drive electronics for the WSO Ultraviolet Spectrograph Subsystem (WUVS). WSO-UV is a major Russian-led international collaboration to develop a large space-borne telescope and instrumentation to study the universe at ultraviolet wavelengths between 115 nm and 310 nm. The WUVS is led by the Institute of Astronomy of the Russian Academy of Sciences. WUVS consists of two high resolution spectrographs covering the far-UV range of 115-176 nm and the near-UV range of 174-310 nm, and a long-slit spectrograph covering the wavelength range of 115-305 nm. RAL Space is providing the camera electronics that will interface with the custom-designed CCD sensor and cryostat assembly developed by e2v technologies (UK).

This paper describes the implementation of DCDS within the constraints of a space-based application that imposes challenging technical requirements. We discuss the key design trade-offs with particular emphasis on those relating to the baseline readout noise requirement of < 3 electrons rms read out at 50 kpixels/s. The results presented illustrate the performance achieved by this novel design now that the CEB has passed the critical design review. Finally, we present our plans for the next stage in this development including the use of weighted averaging for even lower readout noise in the future.

I. INTRODUCTION

World Space Observatory Ultraviolet (WSO-UV) is a major Russian-led international collaboration to develop a large space-borne 1.7 m Ritchey-Chrétien telescope and instrumentation to study the universe at ultraviolet wavelengths between 115 nm and 320 nm. There are a number of key science drivers for the mission, including the study of galaxy formation, the evolution of the Milky Way and the atmospheres of extrasolar planets [1].

There are two primary sets of instrumentation on the satellite [1]; the Field Camera Unit (FCU) and the WSO Ultraviolet Spectrographs (WUVS). The FCU is a UV imager with two channels; a far ultraviolet (FUV) channel covering 115-175 nm wavelengths and a near ultraviolet (NUV) channel covering 185-320 nm wavelengths. The WUVS instrument set consists of three spectrographs:

- Vacuum Ultraviolet Echelle Spectrograph (VUVES): 115-176 nm, R=50000
- Ultraviolet Echelle Spectrograph (UVES): 174-310 nm, R=50000
- Long Slit Spectrograph (LSS): 115-305 nm, R=1000

The custom-designed CCD sensors and cryostat assemblies for the WUVS instrument are being provided by e2v technologies (UK). STFC RAL Space is providing camera electronics boxes (CEBs) which house the CCD drive electronics for each of the three WUVS channels.

To meet the science drivers for the mission, the sensor and drive electronics solution must be capable of achieving less than 3 e- rms noise at 50 kHz pixel frequency whilst maintaining a high dynamic range of at least 10000:1 [2]. The drive electronics must be suitable for operation in the spacecraft environment with a minimum operational lifetime of 5 years and an optional extension up to 10 years.

The full range of science and engineering mode operation requires that the CCD drive electronics is able to operate in a number of flexible readout modes. These include provision for readout of the CCD at pixel frequencies of 50 kHz, 100 kHz and 500 kHz with both single pixel readout and 2x2 pixel binning. In addition, the CCD clock sequencing required for the LSS channel differs slightly from the UVES and VUVES channels due to the different spectral layout on the sensor [3].

This paper describes the design elements and key features of the CCD drive electronics for low-noise CCD readout in space applications with particular emphasis on the digital correlated double sampling (DCDS) method used.

The latest results of the engineering model tests are presented including detailed analysis of the video performance including noise, linearity, crosstalk and transient response.

II. DESIGN OVERVIEW

The WUVS CCD camera sub-system is shown in Fig. 1. The cryostat assembly, provided by e2v technologies (UK), consists of a CCD272-64 CCD inside a vacuum enclosure. An Interconnect Module (ICM) is mounted directly to the outside of the CCD enclosure and is linked to the main Camera Electronics Box (CEB) via a short electrical harness. All command and data packets from/to the spacecraft are carried via primary and redundant SpaceWire links. Primary and redundant power to the sub-system is supplied at 27 V.

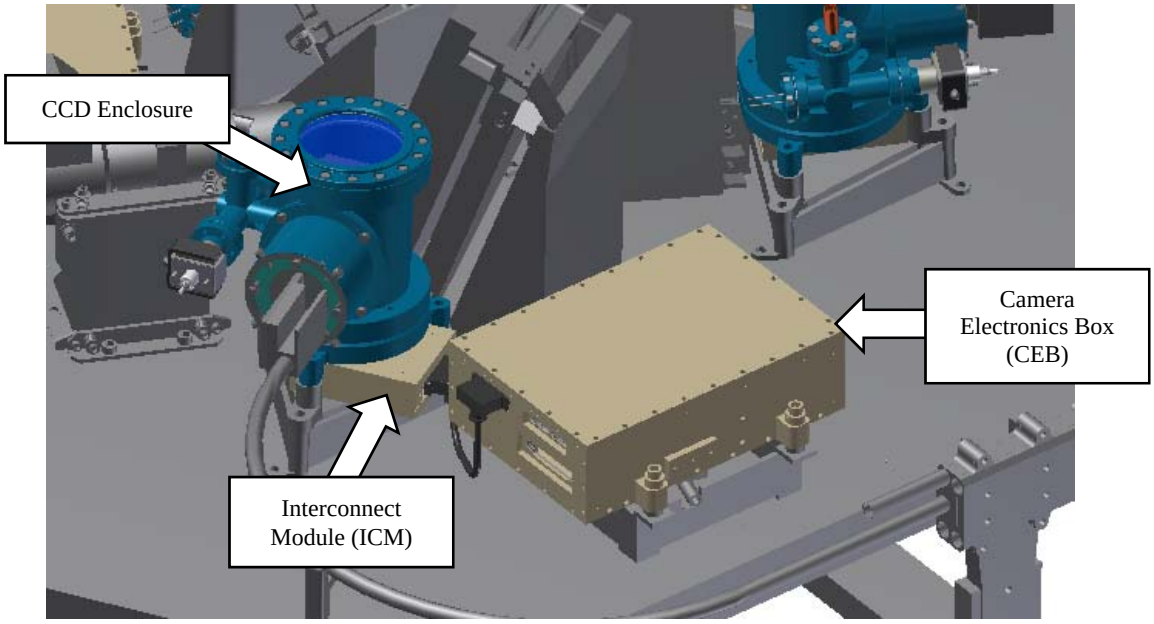

Fig. 1. WUVS CCD camera sub-system (image credit: e2v).

The drive electronics have been designed to be radiation tolerant to both total ionising dose (TID) and single event effects (SEE) through the selection of space-qualified components and, where required, further up-screening qualification. All hardware has been designed to survive the expected levels of vibration, shock and temperature variation during integration, launch and operation of the satellite and the design will be subjected to a full environmental testing qualification programme prior to delivery.

The ICM is mounted directly to the outside of the vacuum enclosure and forms an important link between the CEB and CCD. The ICM provides decoupling for the CCD bias voltages, impedance-matching and rise/fall-time control of the CCD clock waveforms in order to minimise the impact of the harness. The ICM also includes JFETs that are used to buffer and drive the CCD video signals along the harness.

The CEB provides a SpaceWire and power interface to the spacecraft and implements the low-noise video digitisation, CCD bias voltage generation and CCD clock generation electronics. It is formed of three major sub-assemblies; the power supply, bridge card and CCD camera card. A detailed block diagram of the CEB electronic architecture is shown in Fig. 2.

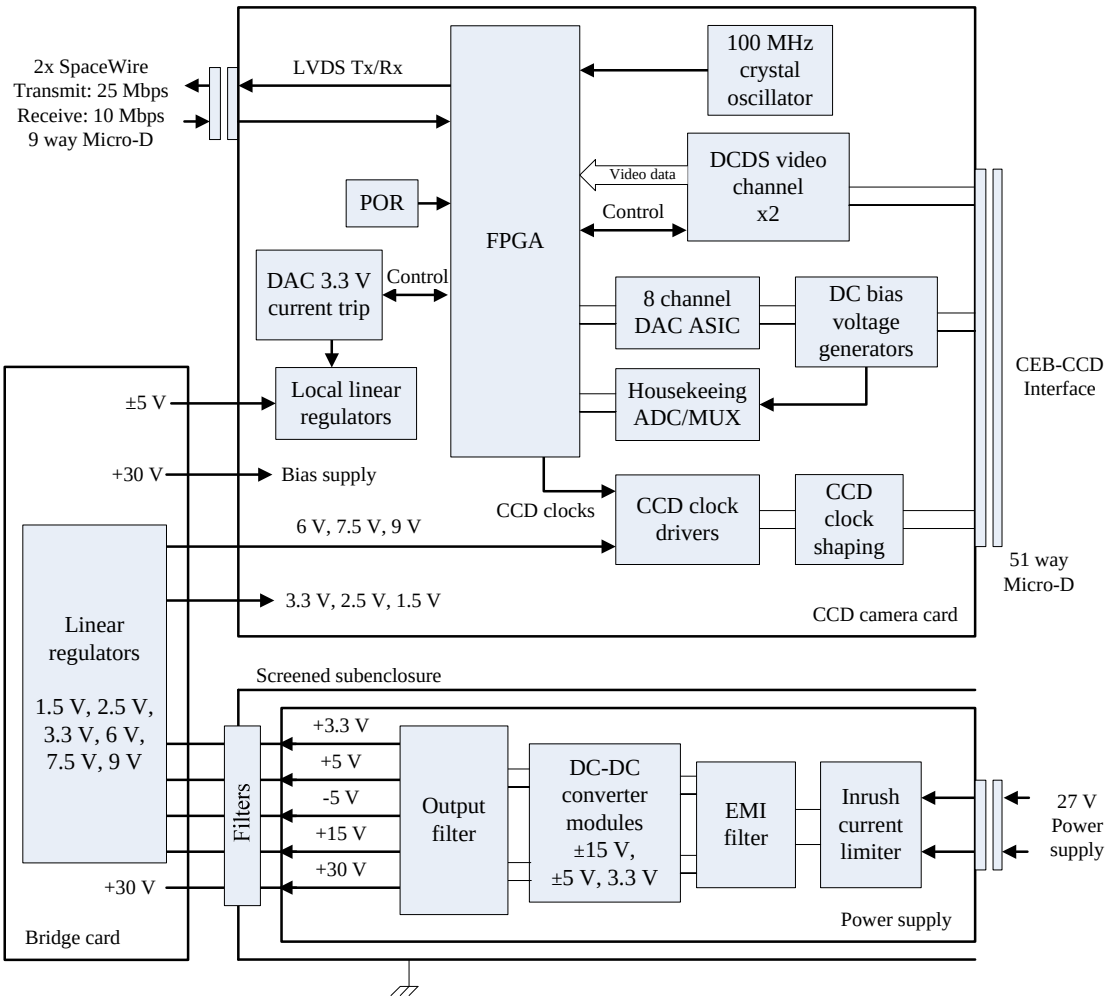

Fig. 2. CEB block diagram showing the internal electronic architecture.

The CEB power converter circuitry is contained within a screened sub-enclosure at the base of the unit to limit electrical interference from the switching DC-DC converters coupling into sensitive analogue circuitry elsewhere in the CEB. Running from a prime/redundant 27 V bus, the power converter sub-system provides in-rush current limiting, current-trip protection, EMC input filtering, DC-DC conversion and secondary rail output filtering. Five discrete DC-DC converter modules are configured to provide +3.3 V, +5 V, -5 V, +15 V and +30 V secondary power rails. The converter outputs are filtered, decoupled, and passed to the CEB bridge card through filtered feedthroughs with separate supplies for key analogue and digital functionality.

The bridge card contains multiple linear voltage regulators to generate the additional voltage supplies required by the CEB. This includes the CCD clock driver and FPGA supply voltages alongside additional general purpose analogue and digital supply rails. The flexi-rigid PCB design allows the card to bend through 90° and extend up the back wall of the CEB enclosure such that all of the supply voltages are available on a single backplane connector. The coupled power supply and bridge card unit has been designed as an adaptable space-qualified power solution for CCD drive electronics allowing easy integration of future drive electronics cards with minimal re-design effort.

The CCD camera card sits above the power supply and bridge card and provides the majority of the specialist functionality to interface with the CCD and the spacecraft. The core logic functionality of the CEB is implemented on a radiation-tolerant, flash-based reprogrammable FPGA. The control and data communications link with the spacecraft is a primary/redundant SpaceWire (ECSS-E-ST-50-12C) serial interface, featuring a low-voltage differential signalling (LVDS) driven SpaceWire serial data link with a programmable transmit rate.

The CCD interface is a 51-way micro-D connector that enables all CCD clocks, biases and video signals to be routed on a single, internally screened, harness. Provision has been made in the CEB design to ensure that it is suited to as many CCD applications as possible with, for example, the provision of electronics for additional clocking phases.

The main CEB enclosure dimensions are 150 mm (width) x 220 mm (length) x 65 mm (height). The CEB is mounted to the spacecraft using four mounting bolts through feet at the base of the side panel. The total width including the mounting feet is 185 mm. The EM CEB is shown in Fig. 3.

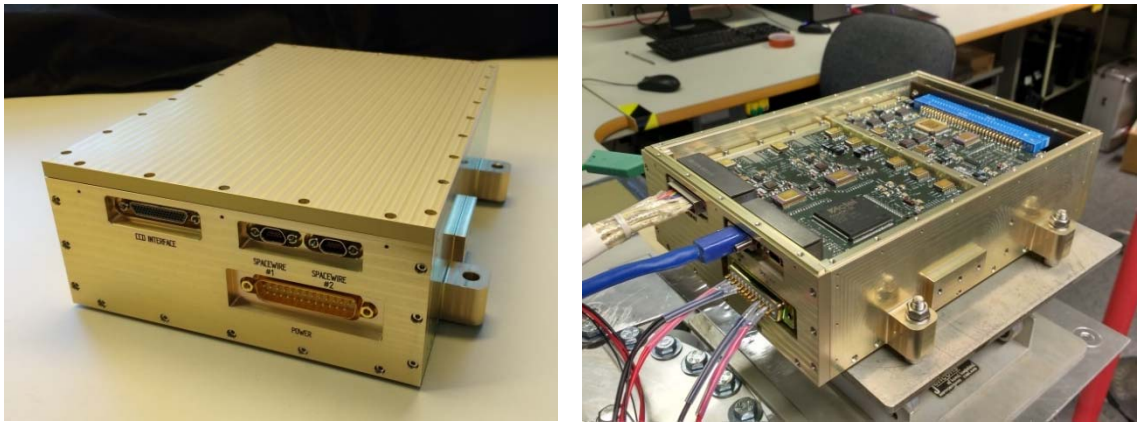

Fig. 3. Photographic overview of EM CEB testing. Assembled EM CEB (left), system level testing with the top panel removed showing the CCD camera card (right).

III. DCDS DESIGN

The WUVS CCD provides both real and dummy outputs which offer the possibility of common-mode noise rejection, reduced susceptibility to electromagnetic interference and inherent attenuation of clock feed-through on the video signals. The CEB's video front-end electronics interfaces with the high-voltage CCD output using an AC couple and a voltage-clamp DC restore technique. The resultant signals are amplified and buffered by the first-stage operational amplifiers before a fully-differential amplifier is used to drive a high-speed high-performance ADC. The CEB contains two video channels, referred to as channel 1 and 2 within this work, to enable simultaneous readout from two CCD ports.

Low-noise correlated double sampling (CDS) and digitisation of the CCD video signals is implemented using digital correlated double sampling (DCDS) [5]. This technique differs from traditional CDS performed in the analogue domain and enables variable digital sampling and averaging of the CCD's video signal.

To achieve this, the 14-bit ADCs in the CEB continuously sample the video signal at a rate of 25 MHz such that the entire pixel waveform, including settling and clamp periods, is digitised. This enables multiple valid samples to be obtained during the reference and signal periods of the pixel waveform, as illustrated in Fig. 4. When operating at a pixel frequency of 50 kHz the CEB obtains around 150 valid samples during each period.

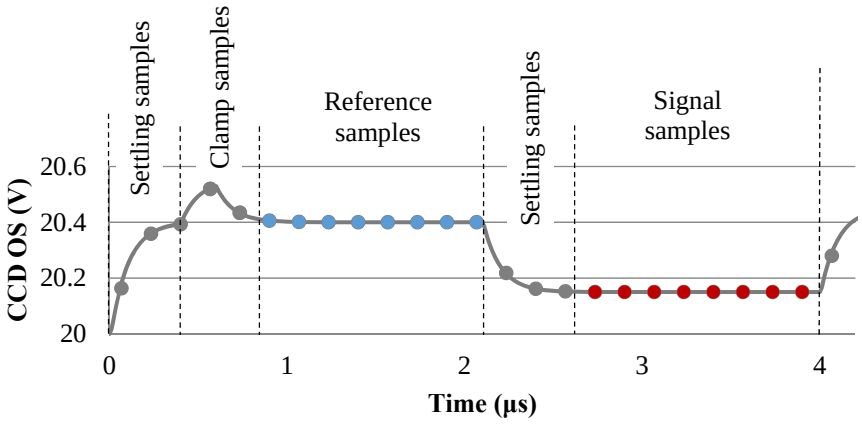

Fig. 4. Indicative plot of a pixel waveform showing the signal settling period, clamp period and example locations for the reference (blue) and signal (red) samples.

To minimise design complexity, a simple averaging filter function (1) is implemented in the CEB's FPGA that subtracts the average of the signal samples from the average of the reference samples.

$$P = \frac{1}{n}\sum_{i=1}^{n} r_i - \frac{1}{n}\sum_{i=1}^{n} s_i \quad (1)$$

where

r_i = reference samples

s_i = signal samples

n = number of reference and signal samples

P = resulting pixel value

The pixel value is calculated with high precision and then rounded to either 14 or 16 bits. Due to the low readout noise at 50 kHz (< 1 LSB at 14 bits), there may be a small increase in system noise due to the quantisation error when operating with the 14-bit data format. However, the 14-bit data format does allow additional flags to be sent with the pixel, including an end-of-line flag and an error-condition flag. The user may select either mode depending on project requirements.

Assuming that all noise sources are white noise then the averaging function reduces the total noise on the resultant pixel value in proportion to the square root of the number of samples. This has an impact on the overall design of the WUVS CCD camera sub-system as the number of reference and signal samples that are available directly influences the noise reduction that is possible. When operating at higher pixel frequencies, such as 500 kHz, the number of samples available for each pixel is greatly reduced limiting the effectiveness of the DCDS noise reduction.

The number of available samples is also limited by the effect of the CCD clocks coupling into the video signal. One of the key science modes for the WUVS application is 2x2 binning, requiring a greater number of CCD clock transitions within the pixel waveform. The CCD clock transitions couple into the video waveform generating small perturbations on each clock edge. To date, the samples within this period of the waveform have not been used to minimise the risk that performance will be degraded. The camera electronics has also been designed to allow specific samples within the pixel waveform to be excluded or included in the averaging function, allowing the DCDS algorithm to be optimised and tuned at any stage during development or operation.

A further trade-off has been required between design complexity and video settling time. Previous work [6] has found that using samples from the settling period of the pixel waveform may degrade the noise performance and therefore it is important to avoid using these samples for the DCDS averaging. As a consequence, the video harness has been kept as short as possible within the mechanical constraints of the system. Furthermore, JFET buffers included in the ICM to drive the harness, enable faster settling time of the CCD video signal and minimise the number of samples lost to settling time.

While the WUVS programme is ongoing, a number of tests have already been carried out to characterise the performance of the DCDS system including the system noise and camera electronics linearity, adjacent pixel crosstalk and inter-channel crosstalk. These results are described in the following section.

IV. DCDS CHARACTISATION AND RESULTS

A cooled CCD test chamber has been used to characterise the noise performance of the drive electronics for all of the required pixel frequencies (50 kHz, 100 kHz and 500 kHz) with both 1x1 binning and 2x2 binning. The system gain of both CCD ports was measured for each readout mode using a photon transfer curve. The gain measurements obtained in each mode with the test CCD were typically in the region of 3.2 to 3.3 e^-/ADU. The test system was also used to capture a dark image in each readout mode and the standard deviation of the CCD's underscan region was measured to obtain the system noise in ADU rms. These figures were used, alongside the measured system gain, to calculate the system noise performance for each operating mode.

In addition, a noise model previously described in [5] has been adapted and applied to the WUVS DCDS system. The model has been used to optimise the DCDS performance within the significant constraints of the available components for satellite applications. The modelled noise results also provide a useful benchmark against which the measured noise results can be compared.

Fig. 5 and Fig. 6 show the measured and modelled system noise for video channel 1 and 2 of the test CCD operating at 50 kHz, 100 kHz and 500 kHz pixel frequencies with 1x1 pixel binning and 2x2 pixel binning respectively.

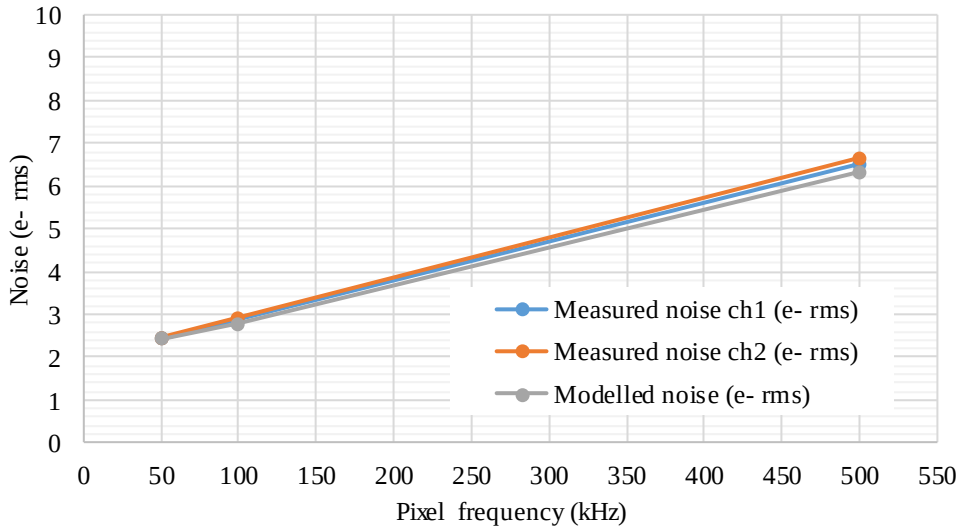

Fig. 5. Modelled and measured system noise plotted against pixel frequency when using 1x1 pixel binning.

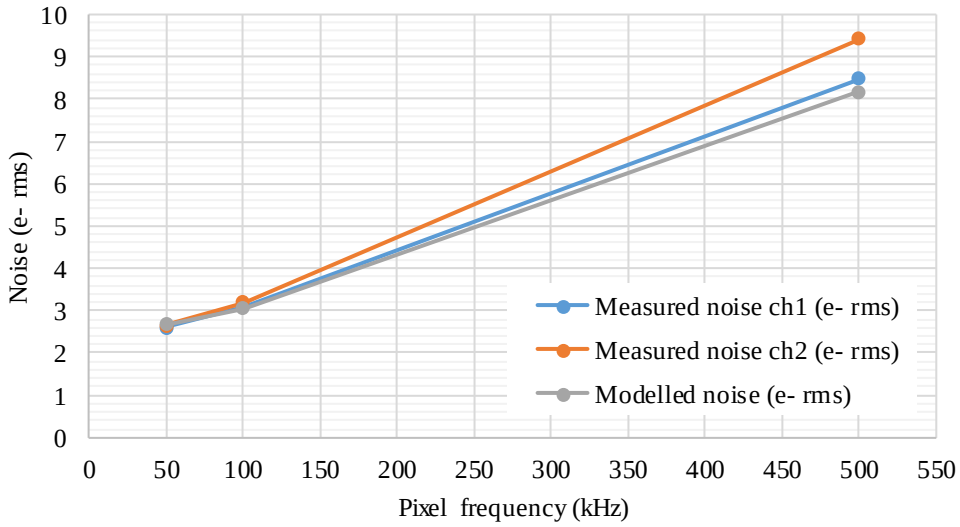

Fig. 6. Modelled and measured system noise plotted against pixel frequency when using 2x2 pixel binning.

As expected, the system noise increases as the pixel frequency increases. The average noise across both ports at 50 kHz was 2.44 e- rms with 1x1 binning and 2.64 e- rms with 2x2 binning. These results demonstrate that the drive electronics, in conjunction with the test CCD from e2v, are capable of achieving the key WUVS noise specification of less than 3 e- rms noise at a pixel frequency of 50 kHz.

Generally, the measured noise results shown in Fig. 5 with 1x1 binning correlate well with the model results. There is a slight deviation at 500 kHz due to the limited sampling time and resulting trade-offs that are required. Effects due to the settling samples and CCD clocks coupling into the video waveform are not modelled and these are likely to be causing the additional noise seen in the high pixel frequency case. With 2x2 binning a larger proportion of the pixel period is required for clocking the CCD serial register and therefore the quantity and timing of the DCDS samples are further constrained. This results in a larger deviation between the measured and modelled results at 500 kHz as shown in Fig. 6. Nonetheless, the 2x2 binning results at 50 kHz and 100 kHz do correlate well with the model.

The CEB's analogue front-end is configured for a CCD input signal range of approximately 250 mV which equates to a CCD responsivity of 8.5 µV/e- and a full well capacity of 30 ke-. A CCD signal emulator has been used to feed an emulated ramp image into the CEB consisting of 32,000 rows of pixels covering the full input

range. The pixel value presented to the CEB was gradually increased row-by-row from zero signal level to full-scale. The non-linearity has been characterised using a best fit line and the variation from this line is presented as a percentage of the full CCD input voltage range. The peak deviation from the best fit line is shown in Table 1, which is well within the target requirement for the electronics of 1%.

Table 1. CEB linearity shown as the peak deviation from a best fit line expressed as a percentage of the full CCD input voltage range.

CEB video port	Linearity
Channel 1	+0.13%/-0.10%
Channel 2	+0.16%/-0.11%

The first type of crosstalk that was characterised on the CEB is the adjacent pixel crosstalk, or transient response, where the signal on one pixel affects the digitised value of the adjacent pixel. A CCD signal emulator was used to feed transients into the CEB's video inputs such that, during each row of a test image, specific pixels would see a full-scale input signal whilst the adjacent pixels were fed zero-scale input signals. Applying a large transient in this way allows the effect of the previous pixel's value on the current pixel to be measured. The deviation from the ideal pixel value is shown in Table 2 with the results expressed as a percentage of the transient magnitude.

Table 2. CEB electronics contribution to adjacent pixel crosstalk.

CEB video port	Transient direction	Adjacent pixel crosstalk
Channel 1	High to low transients	0.03%
	Low to high transients	0.05%
Channel 2	High to low transients	0.03%
	Low to high transients	0.01%

The second type of crosstalk that has been characterised is inter-channel crosstalk. As the CEB contains two independent video channels, large transients on one port can influence the digitised data on the other port. To measure the inter-channel crosstalk a CCD signal emulator was used to feed full-scale transient signals into one port whilst the real and dummy inputs were shorted together on the other port. The inter-channel crosstalk observed is shown in Table 3.

Table 3. CEB electronics contribution to inter-channel crosstalk.

CEB video port		Inter-channel crosstalk
Aggressor	Victim	
Channel 1	Channel 2	-40.9 ppm
Channel 2	Channel 1	-6.8 ppm

The results for both types of crosstalk are significantly within the target specification and are insignificant within the context of the 3% system specification.

V. CONCLUSIONS AND FUTURE PLANS

The latest results from testing the DCDS implementation within the WUVS camera electronics have been described. The results demonstrate the excellent performance currently being achieved using this method with very low noise of approximately 2.5 e- rms at 50 kHz pixel frequency alongside excellent linearity and cross-talk. The ability to dynamically adjust the CCD readout frequency over a wide range has also been demonstrated allowing the CCD readout time to be traded for readout noise at any stage of operation. Finally, a good correlation has been shown between the measured and modelled results providing good confidence in the future performance of this technology.

Previous work [6] has demonstrated that the use of DCDS weighted averaging may further reduce the system noise at low pixel frequencies due to the attenuation of 1/f noise. Whilst a 50 kHz pixel frequency is on the borderline of the frequency range at which this technique is most effective, it is possible that some reduction in

system noise will be observed with this method. Once test hardware becomes available this will be tested to quantify any performance gain achieved and determine whether this feature may be suitable for our low-noise, high performance cameras of the future.

VI. ACKNOWLEDGEMENTS

The development of the CCD drive electronics would not have been possible without the significant contributions made by all members of the WUVS project team at STFC RAL Space. In addition, thanks are due to the project team at e2v for the provision of the imaging sensors used during the testing and characterisation of the drive electronics and for their continued project support.

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