Inspection and metrology for through-silicon vias and 3D integration

Andrew C. Rudack
SEMATECH, 257 Fuller Road, Suite 2200, Albany, NY, USA 12203

ABSTRACT

3D IC integration employs advanced interconnect technologies including through-silicon vias (TSVs), bonding, wafer thinning, backside processing and fine pitch multi-chip stacking. In 2013, Mobile Wide I/O DRAM is expected to be one of the first high volume 3D IC applications. Many of the manufacturing steps in TSV processing and 3D integration can complicate inspection and metrology. This paper reviews a typical via-mid flow emphasizing the inspection and metrology challenges inherent in 3D integration. A preliminary look at the 2011 ITRS roadmap for 3D interconnect metrology is presented, including the gaps in currently available inspection and metrology tools.

Keywords: 3D, 3D integration, 3D Stacked IC, through-silicon via, TSV

1. INTRODUCTION

Inspection and metrology for through-silicon vias (TSV) and 3D integration is a relatively new addition to the SPIE Advanced Lithography Metrology conference. Starting in 2010, an overlay paper demonstrating IR microscopy as an early predictor for electrical yield in bonded wafer pairs[1] was presented. 2011 saw an author presenting on 3D IC inspection and metrology[2]. The 2012 metrology conference offered an entire 3D inspection and metrology session with six authors presenting on a variety of subjects including void growth and detection in copper plated TSVs[3,4], creative optical techniques for etched TSV depth and profile metrology[5,6], warped wafer characterization for 3D interconnect[7] and an overview of in-line metrology tools for 3D interconnect processes[8].

Researching inspection and metrology for TSV and 3D integration, the SEMATECH 3D Interconnect program has been operating at the College of Nanoscale Science and Engineering (CNSE) in Albany, NY since 2007. The 3D program leverages a complete, state-of-the-art 300mm CMOS wafer line. Wafer starts in the CNSE fab deliver substrates ready for SEMATECH's 3D integration experiments, using tools acquired or adapted specifically for 3D interconnect and TSV processing:

- TSV etcher capable of 10:1 – 20:1 high aspect ratio (HAR) vias
- Multi-cell copper plater capable of filling HAR vias following liner, barrier and seed deposition
- Align/bond tools including wafer-to- wafer, die-to-wafer and die-to-die tools to create bonded wafer stacks using copper and adhesive bonding techniques.
- Spin/bake tool for applying both permanent and temporary bonding adhesives to enable materials characterization
- 3D metrology tools including scanning acoustic microscope (SAM), infrared (IR) microscope and thickness/bow/warp monitor (capacitance probe)
- All surface inspection tool capable of monitoring top, bottom and wafer-edge bevel
- TSV copper-plated void metrology
- Wafer thinning tools including back grinder and wet hood for cleans and chemical thinning
- Lithography coat/develop track and exposure tools

Adding 3D-specific process tools to CNSE's CMOS tool set has enabled SEMATECH to establish a 3D research and development center that supports the entire 3D value chain: materials characterization, unit process development, tool

Metrology, Inspection, and Process Control for Microlithography XXVI, edited by Alexander Starikov,
Proc. of SPIE Vol. 8324, 832403 · © 2012 SPIE · CCC code: 0277-786X/12/$18 · doi: 10.1117/12.920301

development, tool hardening, integration, yield verification, early reliability learning, roadmap development, standards development and cost modeling.

2. INTERNATIONAL TECHNOLGY ROADMAP FOR SEMICONDUCTORS (ITRS)

2011 marks the first year the ITRS[9] update included the specific challenges of TSV and 3D interconnect metrology[10], which are reflected in SEMATECH's 3D integration. SEMATECH is currently base-lining a 5 micron diameter, 50 micron deep (10:1 AR) TSV, with a 2 micron diameter, 40 micron deep (20:1 AR) TSV under development. Both integrations will achieve a bonding overlay accuracy of ≤ 1.0 micron (Table 1).

Table 1. 2011 ITRS for 3D stacking and TSV

GLOBAL LEVEL, WTW, DTW, or DTD 3D stacking	2009-2012	2012-2015
Minimum TSV diameter	4-8 µm	2-4 µm
Minimum TSV pitch	8-16 µm	4-8 µm
Minimum TSV depth	20-50 µm	20-50 µm
Maximum TSV aspect ratio	5:1-10:1	10:1-20:1
Bonding overlay accuracy	1.0-1.5 µm	0.5-1.0 µm
Minimum contact pitch (thermocompression)	10 µm	5 µm
Minimum contact pitch (solder or SLID)	20 µm	10 µm
Number of tiers	2-3	2-4
INTERMEDIATE LEVEL, WTW 3D stacking	**2009-2012**	**2012-2015**
Minimum TSV diameter	1-2 µm	0.8-1.5 µm
Minimum TSV pitch	2-4 µm	1.6-3 µm
Minimum TSV depth	6-10 µm	6-10 µm
Maximum TSV aspect ratio	5:1-10:1	10:1-20:1
Bonding overlay accuracy	1.0-1.5 µm	0.5-1.0 µm
Minimum contact pitch	2-3 µm	2-3 µm
Number of tiers	2-3	8-16 (DRAM)

3. VIA-MID INTEGRATION

For TSV and 3D integration, SEMATECH uses its 403AZ reticle test vehicle, which supports 20 electrical tests including via chains, overlay verniers, comb structures, Kelvin structures, electro-migration, thermal and stress tests.

SEMATECH's 3D integration uses a via-mid approach. TSVs are etched into 775 micron full thickness 300mm wafers. Etch depth is determined by etch time, etcher across-wafer uniformity, and pattern density. Typically, the via-mid approach will insert TSVs after transistor formation and before TSV wafer rotation and bonding to a carrier. Subsequent wafer backside grinding and chemical thinning reveals TSVs from the bottom of the etched and filled via. Good TSV etch depth control and an algorithm to understand all contributions to the TSV reveal are necessary to reliably expose vias for subsequent electrical contact and acceptable yield.

Via-mid integration will challenge TSV and 3D metrology with HAR features ≥ 10:1. Opaque materials such as copper, silicon and materials with high extinction coefficients often require sub-surface imaging as visible and e-beam techniques do not work. Lithography tools need to adopt different alignment techniques using backside marks, buried marks (requiring IR alignment hardware), or features that become visible in silicon through the TSV reveal. Via-mid integration also introduces processing challenges when using front-end tools following traditional back-end tools such as bonders and back-grinders (Figure 1).

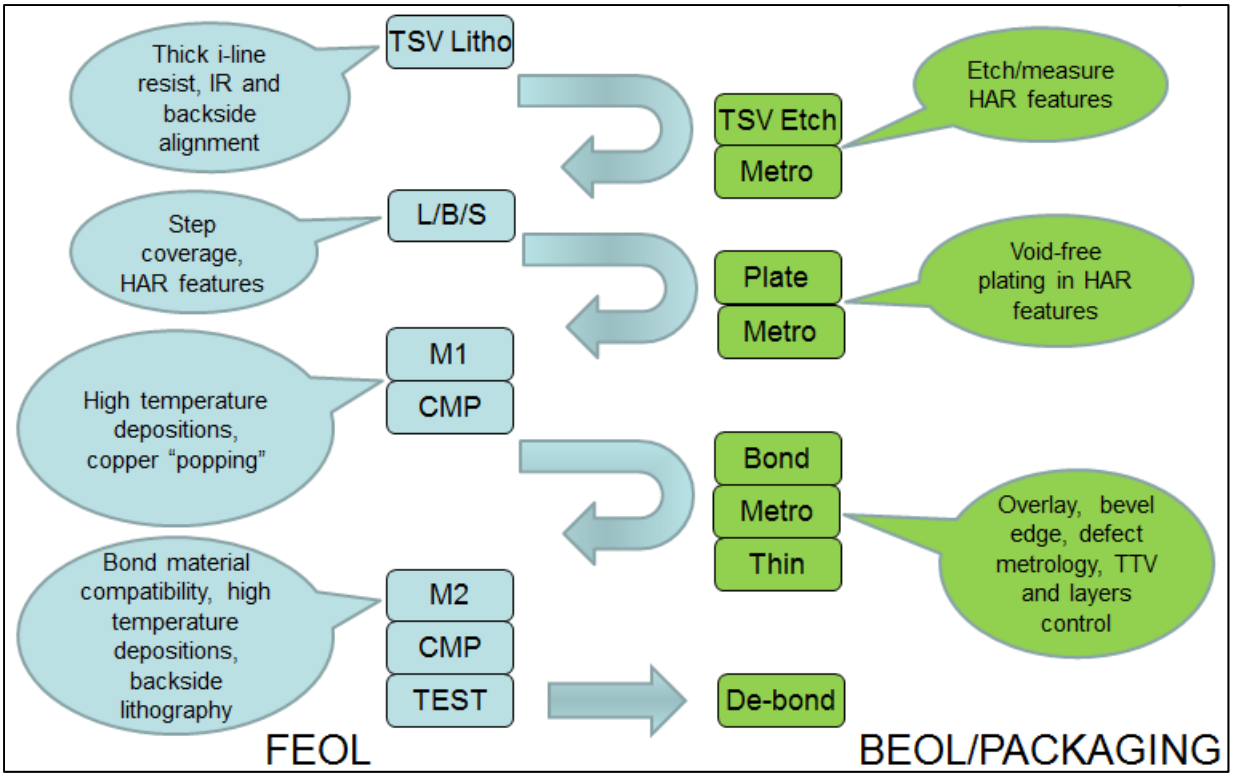

Figure 1. Process flow for via-mid TSV integration. Wafers can move from the front end-of- line (FEOL) to back end-of-line (BEOL) on TSV and traditional packaging tools and return to the FEOL for subsequent processing. Metrology and 3D integration process challenges that result are highlighted.

4. ITRS LISTED CHALLENGES FOR 3D INTERCONNECT METROLOGY [11]

4.1 Bonding overlay

Measurements are typically taken through silicon at the interface of bonded wafer pairs, requiring IR microscopy and overlay metrology software. The IR source can be broad-band, or laser-based. Overlay alignment fiducials are required and wafer space allocated, typically in the kerf area. Overlay metrology is necessary to verify that overlay tolerances will be met for electrical connectivity and to ensure wafer notch alignment for subsequent process tool operations following the bonder (Figure 2).

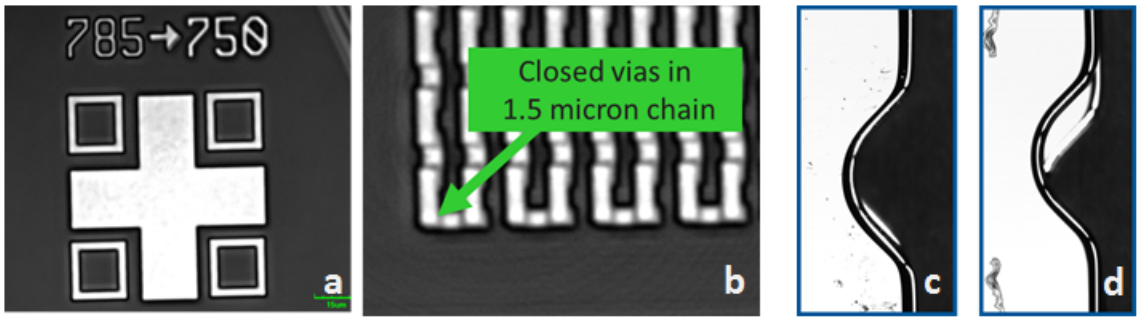

Figure 2. IR microscope image - Alignment fiducial showing good wafer-to-wafer overlay (a). IR microscope image – electrically yielding via chains resulting from good overlay (b).Visible microscope image of properly aligned bonded wafer pair notch (c). Improperly aligned bonded wafer notch can cause process tool wafer pre-aligner issues (d).

4.2 Bonded interface void detection

Bonded wafers must survive subsequent thinning and edge-bevel trimming operations. Metrology is required to assure voiding or adhesive issues at the interface of bonded pairs will not contribute to wafer separation Scanning Acoustic Microscopes (SAMs)can detect voids at the interface of bonded wafers. SAM-induced defectivity can be a concern, but cleaning steps after the grinding should remove those defects.

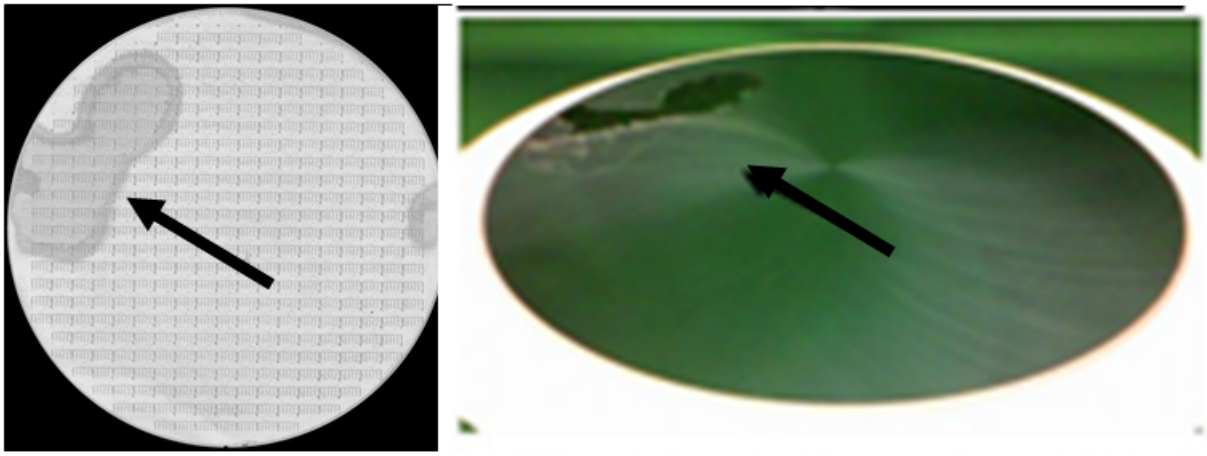

Figure 3. SAM image of bonded wafer pair on left (adhesive issue). Top wafer shredding during grinding is shown on right.

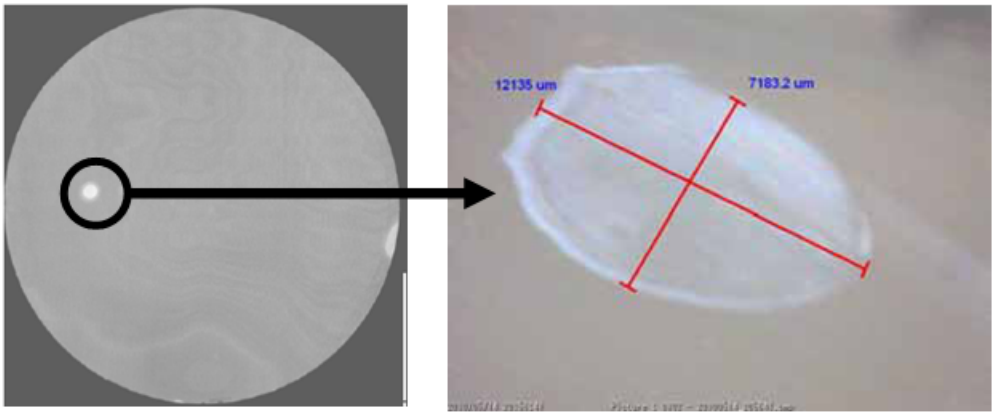

Figure 4. SAM image of bonded wafer with particle-induced void. Silicon bubble delaminated from carrier wafer following wafer thinning.

4.3 Bonded interface defect identification

A metrology tool to support in-line bonded wafer pair defect mapping is required to create Cartesian coordinates for subsequent defect review. Sub-surface imaging to list and characterize defects at the interface of the bonded wafer pair is required. Currently, no defect identification tool to support high-volume manufacturing is available.

4.4 Bonded interface defect review

Defect review tools using IR microscopes are currently available to review and create Cartesian coordinate files (KLARF format) of defects at the interface of bonded wafer pairs. Cartesian coordinate maps can be imported from single wafers

before bonding, and defects later found at the interface of bonded pairs. Defects can be located by KLARF data and viewed, modified or obscured by opaque layers. (Figure 5)

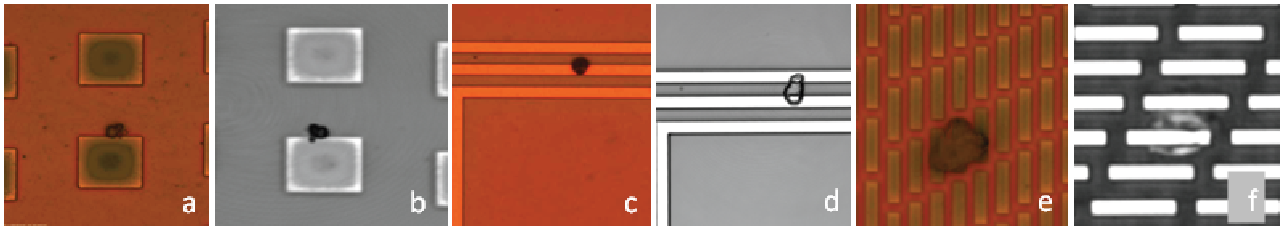

Figure 5. Defect viewed in visible light on single wafer (a), (c), (e). Same defects viewed using IR microscope at interface of a bonded wafer pair (b), (d), (e). Defect (c) modified by bonding now bridges two lines (d) at interface of bonded pair. Defect (e) is partially obscured by opaque layer (f) at interface of bonded wafer pair.

4.5 Edge bevel defects

Edge-bevel inspection identifies edge defects before/after bonding and before/after wafer thinning that could lead to wafer breakage. Wafer thinning necessitates an edge-bevel trim (Figure 6) to control chipping and delamination (Figure 7) during the mechanical thinning process. Several commercial edge-bevel inspection tools are available for high volume manufacturing.

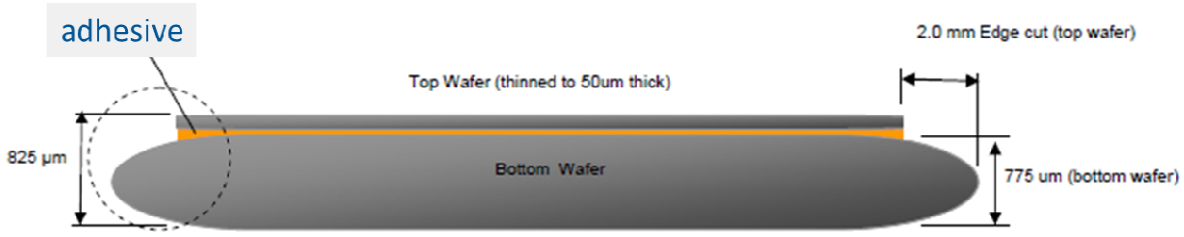

Figure 6. Edge-bevel trim to control edge chipping during wafer thinning.

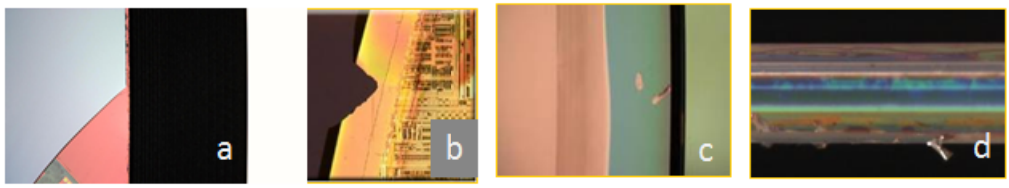

Figure 7. Delamination following wafer thinning (a), edge-bevel chip (b), edge-bevel defects (c), (d).

4.6 Bond strength uniformity

SEMI® standard MS-5[12] defines a micro-chevron test for assessing bond strength uniformity, in addition to four-point bend techniques. Because no in-line metrology tools are currently available to assess bond strength, a destructive, off-line measurement is used instead. Chevrons are etched into a wafer and bonded, then sawn into die for subsequent pull-testing to assess bond strength.

4.7 Bonded wafer pair thickness

Understanding the total thickness variation of the wafer is important in the bonding and thinning operation. Various techniques including capacitance-based metrology, white light interferometry and infrared interferometry can be used. In-line tools to support high volume manufacturing are available.

4.8 TSV etch depth

TSV HARs can exceed 10:1, challenging the use of optical techniques when via diameters are smaller than 5 micron. White light interferometry can be utilized for larger TSVs. Backside interferometry[17] can measure TSVs as small as 0.5 micron in diameter, and is not limited by aspect ratio. Depending on the spot size of the metrology tool, a single TSV can be measured, or farms of TSVs etch depth can be averaged. Several in-line metrology tools are capable of TSV etch depth metrology for high volume manufacturing.

4.9 TSV etch profile

Destructive, cross-sectioning techniques are used to measure TSV etch profiles. Currently, no in-line tool can be used to measure TSVs smaller than 5 micron diameter and >10:1 aspect ratio.

4.10 TSV liner, barrier, seed thickness

Destructive, cross-sectioning techniques are also used to measure liner, barrier and seed thickness. No in-line tool is currently available.

4.11 TSV voids

No in-line tool is available to measure copper plating voids in copper TSVs. Destructive techniques for cross-sectional analysis such as focused ion beam milling (FIB) and scanning electron microscopy (SEM), including whole wafer FIB-SEM are used. Sample preparation for X-ray microscopy is a destructive technique, but allows 3D imaging of TSVs with virtual reconstruction by tomography.

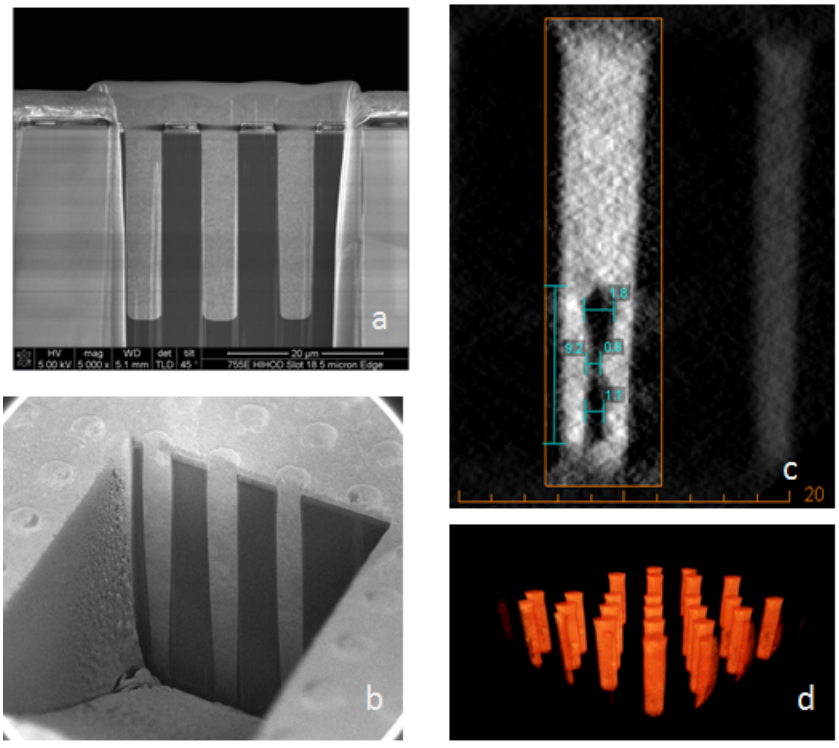

Figure 8. Destructive techniques used for TSV void detection include cross section FIB-SEM (a), whole wafer FIB-SEM (b), X-ray microscope (c) and X-ray computed tomography for 3D virtual reconstructions (d).

4.12 Shape and stress

Numerous technologies currently support wafer shape and stress metrology. Laser deflection, capacitance, interferometer-based, coherent grid systems and chromatic sensors are available for in-line wafer measurements to support high volume manufacturing for bonded wafer pairs. Wafer stress can be calculated by changes in wafer shape. TSV-induced stress in silicon can be measured using Raman spectroscopy.

4.13 Copper nail and pillars (microbumps)

There will be a need for microbump metrology in BEOL manufacturing. Future 3D interconnect technologies will require bonding fine pitch microbumps using solder capped copper pillars or direct copper to copper bonding for stacking circuit blocks in stacked 3D integrations. There is a need for measuring height, diameter and co-planarity for the microbumps used to join the top and bottom circuits in stacked die. Bump metrology techniques like laser triangulation and confocal interferometry are available to measure microbump parameters, but will need adaptation to accommodate smaller microbump diameters.

5.0 SUMMARY

The 2011 ITRS includes 3D interconnect metrology for the first time since the roadmap's inception. It lists 14 key challenge areas and identifies gaps in currently available metrology tools to support TSV and 3D integration. Several challenges are associated with the inability of optical metrology to measure high aspect ratio features and opaque materials, opening opportunities for new tools to be developed and existing capabilities to be adapted to address the gaps in TSV and 3D interconnect metrology.

REFERENCES

[1] Rudack, A., Singh, P., Taylor, J., Mashevsky, V., " IR microscopy as an early electrical yield indicator in bonded wafer pairs used for 3D integration", Proc. SPIE 7638-15 (2010)

[2] Fujimori, Y., Tsuto, T., Kudo, Y., Inoue, T. "A new methodology for TSV array inspection", Proc. SPIE 7971-17 (2011)

[3] Kong, L. et al "Measuring thermally induced void growth in conformally filled through silicon vias (TSVs) by laboratory x-ray microscopy", Proc. SPIE 8324-36 (2012); same volume.

[4] Rudack, A. et al "Through-silicon via plating void metrology using focused ion-beam mill", Proc. SPIE 8324-37 (2012); same volume.

[5] Attota, R. et al. "Three-dimensional nanoscale metrology of CDs and TSVs using the TSOM method", Proc. SPIE 8324-40 (2012); same volume.

[6] Shyu, D. et al. "Measurement of through silicon via etch profile by dark-field optical microscope", Proc. SPIE 8324-38 (2012); same volume

[7] Chang, P., "Wafer level warpage characterization of 3D interconnect", Proc. SPIE 8324-39 (2012);same volume.

[8] Ku, Y. et al. "In-line metrology of 3D interconnect processes", Proc. SPIE 8324-35 (2012); same volume.

[9] International Technology Roadmap For Semiconductors (ITRS) website. http://www.itrs.net/

[10] http://www.itrs.net/Links/2011ITRS/2011Chapters/2011Metrology.pdf

[11] http://www.itrs.net/Links/2011ITRS/2011Chapters/2011Metrology.pdf
3D Interconnect Metrology section, pp. 17-21.

[12] SEMI MS-5-1211, "Test Method for Wafer Bond Strength Measurements Using Micro-Chevron Test Structures", copy available for purchase at www.semi.org

Proceedings from SEMATECH's 3D Metrology Workshops, and additional information on 3D integration are archived on the SEMATECH web at http://www.sematech.org/meetings/archives/3d/index.htm