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Holistic lithography and metrology's importance in driving patterning fidelity

SPIE Advanced Lithography Symposium, Metrology, Inspection and Process Control XXX,
San Jose, 22 February 2016

Martin van den Brink, President and Chief Technology Officer

Content

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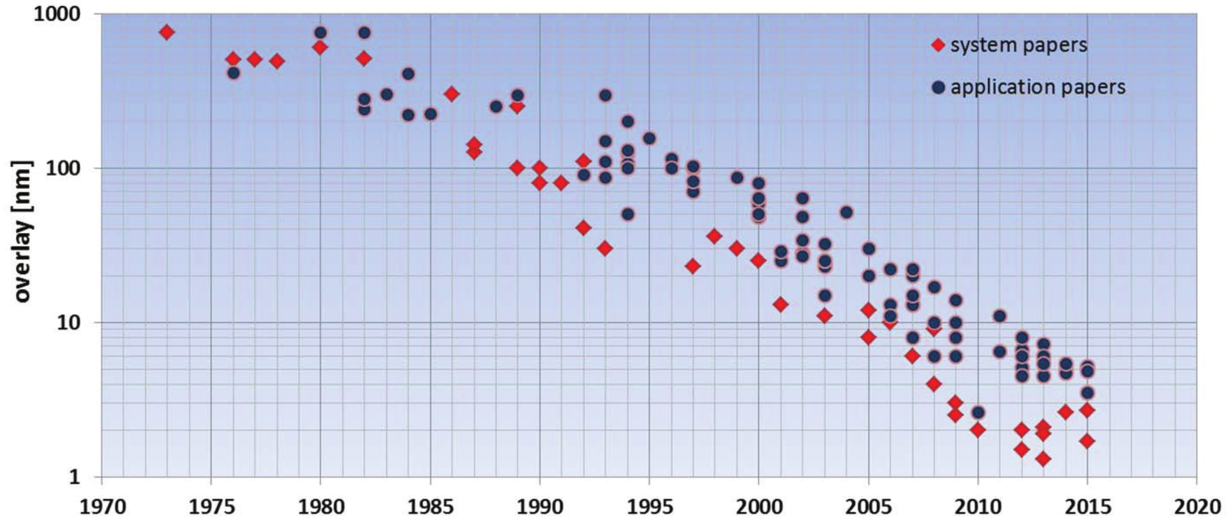
- 43 years overlay metrology in microlithography:
  How did we get here?
  - Stepper metrology improvements
  - Improved correction potential
  - Extend feedback loop outside stepper
- Holistic Lithography: where we are today
- The future of Holistic lithography: where we are going
- Summary

Metrology, Inspection, and Process Control for Microlithography XXX, edited by Martha I. Sanchez, Vladimir A. Ukrainstev
Proc. of SPIE Vol. 9778, 977802 · © 2016 SPIE · CCC code: 0277-786X/16/$18 · doi: 10.1117/12.2225538



43 years overlay: 3 orders of magnitude down¹
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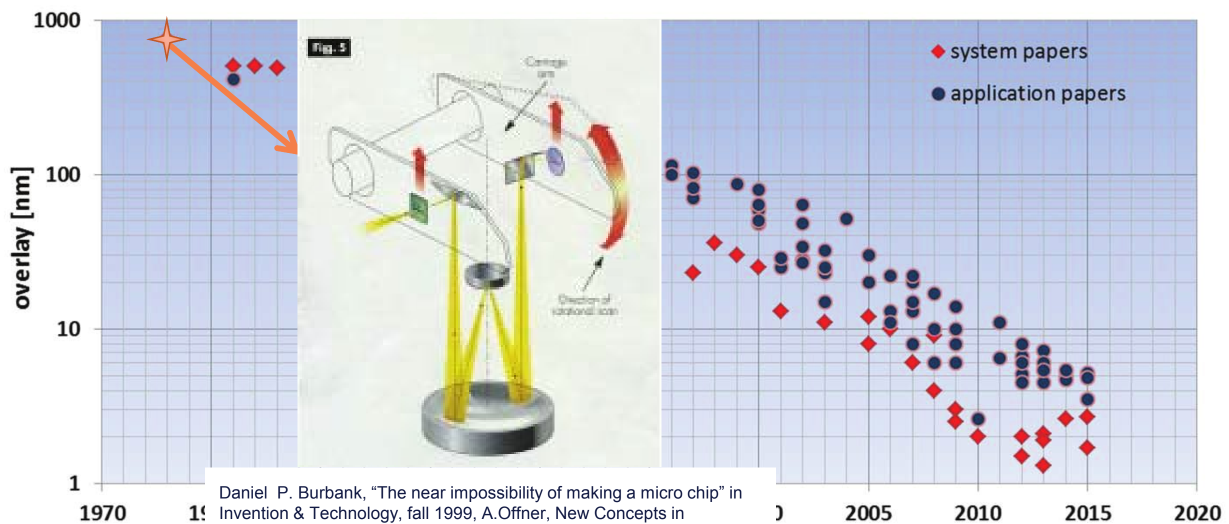
Slide 3
February 2016
1000
100
10
1
overlay [nm]
1970
1975
1980
1985
1990
1995
2000
2005
2010
2015
2020
system papers
application papers
¹Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015



43 years overlay: 3 orders of magnitude down¹
1973: Introducing the first 1:1 wafer stepper, ~0,5 µm overlay
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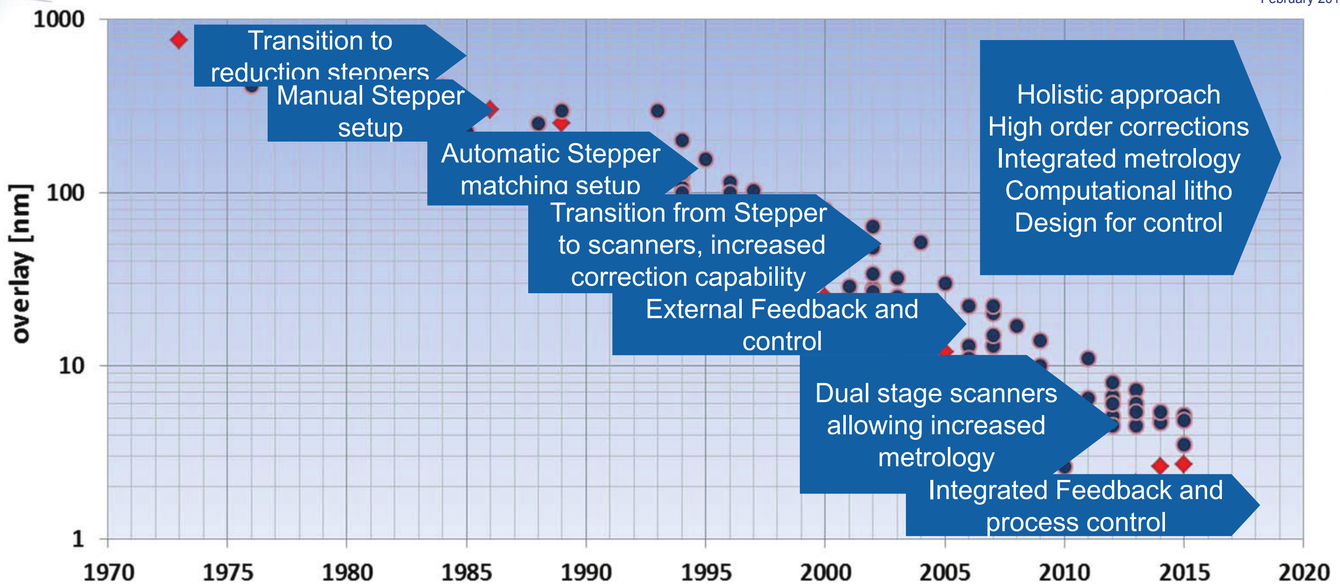
Slide 4
February 2016
1000
100
10
1
overlay [nm]
1970
2005
2010
2015
2020
system papers
application papers
Fig. 5
Daniel P. Burbank, "The near impossibility of making a micro chip" in Invention & Technology, fall 1999, A.Offner, New Concepts in Projection Mask Aligners, Opt. Eng. 14(2), 142130 (Apr 01, 1975). .
¹Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015


43 years overlay: 3 orders of magnitude down¹
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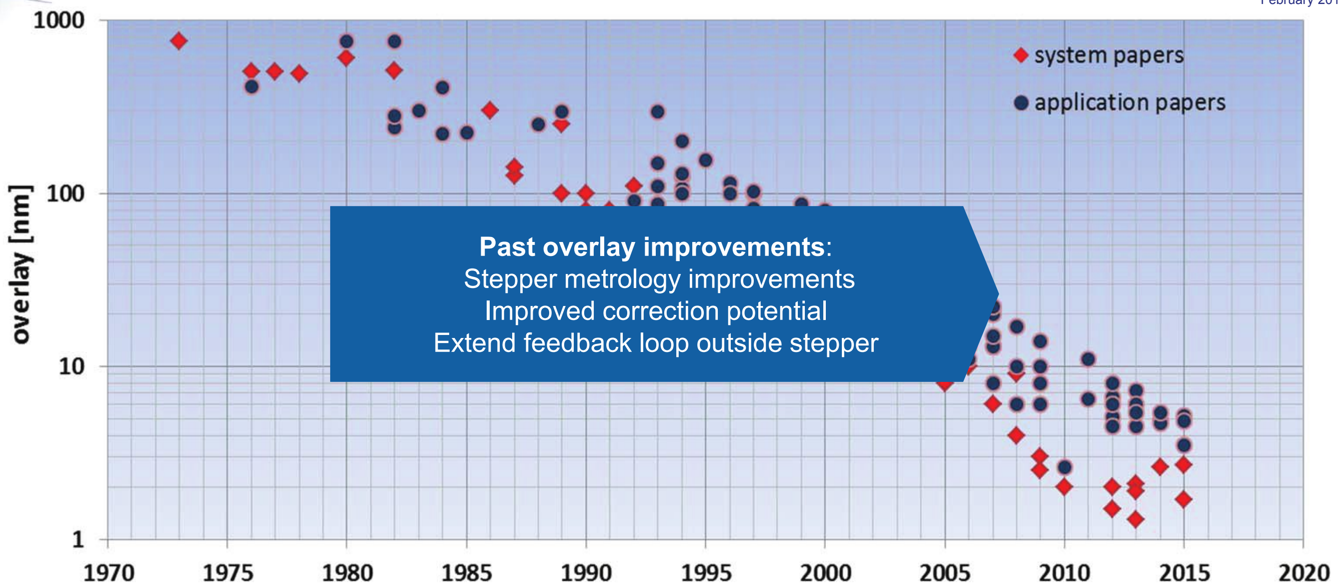
Transition to
reduction steppers
Manual Stepper
setup
Automatic Stepper
matching setup
Transition from Stepper
to scanners, increased
correction capability
External Feedback and
control
Dual stage scanners
allowing increased
metrology
Integrated Feedback and
process control
Holistic approach
High order corrections
Integrated metrology
Computational litho
Design for control
overlay [nm]
1000
100
10
1
1970
1975
1980
1985
1990
1995
2000
2005
2010
2015
2020
¹Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015


43 years overlay: 3 orders of magnitude down¹
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system papers
application papers
Past overlay improvements:
Stepper metrology improvements
Improved correction potential
Extend feedback loop outside stepper
overlay [nm]
1000
100
10
1
1970
1975
1980
1985
1990
1995
2000
2005
2010
2015
2020
¹Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015

43 years overlay: 3 orders of magnitude down, Steppers[1]

1979: 4-parameter reticle to wafer diffraction-based alignment

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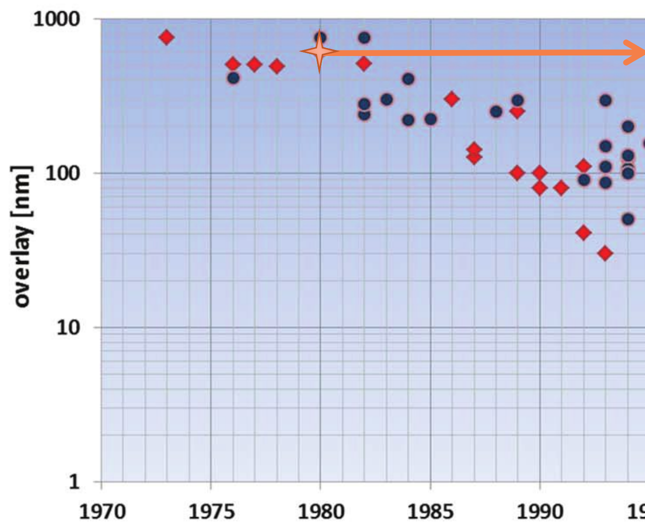

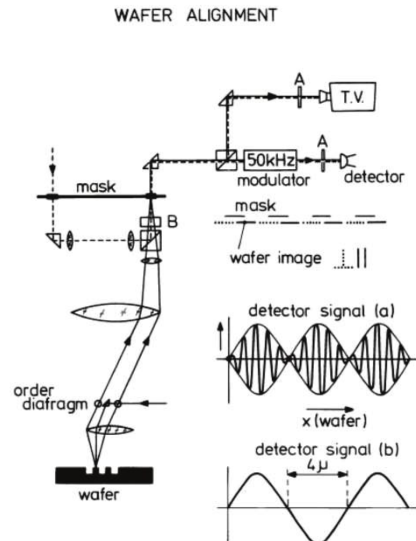

2020

S. Wittekoek, "Step and repeat imaging", Proc. SPIE vol. 334, Optical microlithography I, march, 1982, Gijs Bouwhuis, Stefan Wittekoek, "Automatic Alignment system for optical projection printing", IEEE transactions on electron devices, vol. ED-26, no. 4, April 1979, p 723-728,

[1]Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015

43 years overlay: 3 orders of magnitude down, Steppers[1]

1986: 8-parameter alignment

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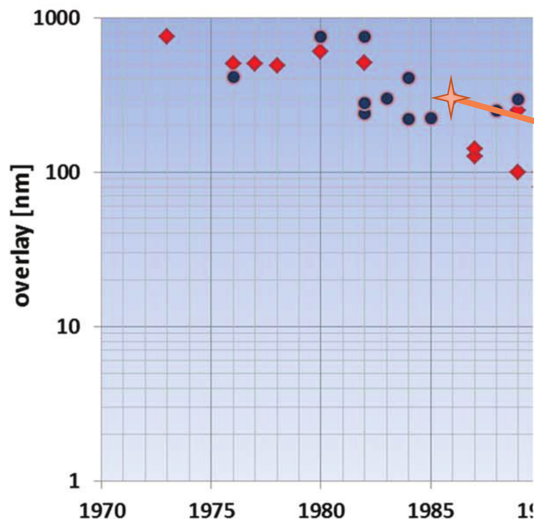

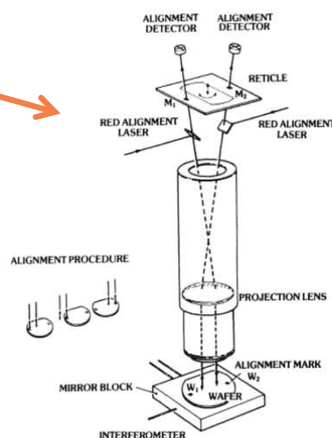

Fig. 3 Simplified scheme of the new dual alignment scheme.

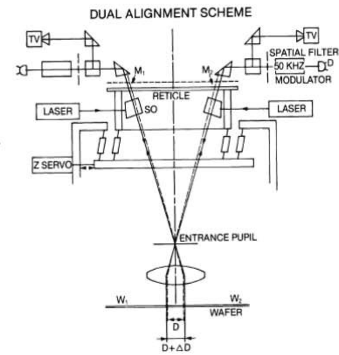

Fig. 4 Detailed scheme of the new dual alignment scheme.

M.A. Van den Brink, H.F.D.Linders, S.Wittekoek, "Direct referencing automatic two-points reticle to wafer alignment using an projection column servo system", Proc. SPIE vol. 633, Optical microlithography V, march, 1986.

[1]Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015

43 years overlay: 3 orders of magnitude down, Steppers[1]

1987-97: Increased correctables on step and scan

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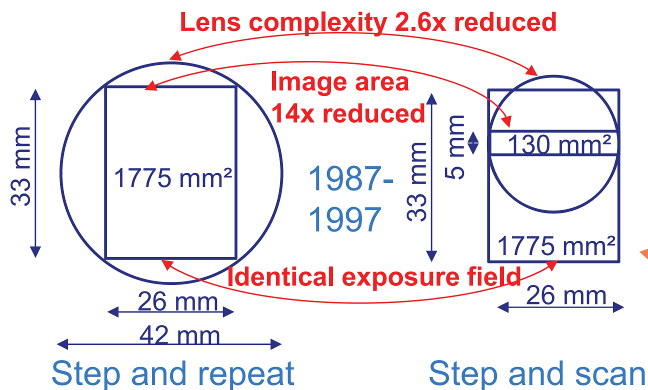

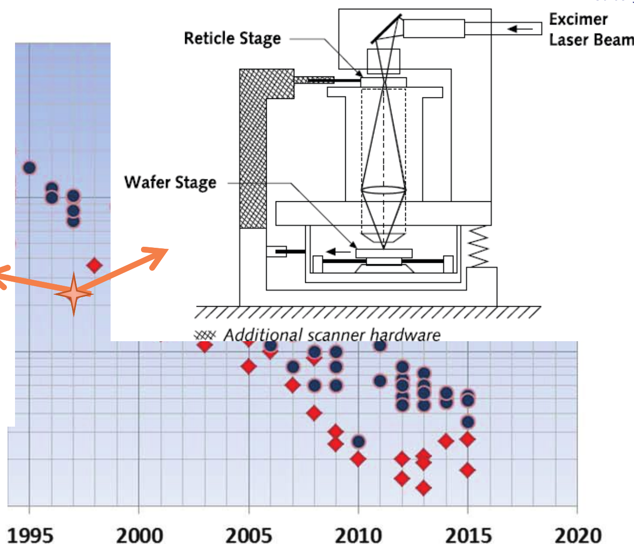

Step and repeat

Step and scan

The small Step and Scan slit enabled imaging and overlay adjustments on millimeter level by adjusting dose, aberration and slit position during scanning

1970 1975 1980 1985 1990 1995 2000 2005 2010 2015 2020

Buckley, C Karatzas, "Step and scan, a system overvieuw of a new lithography tool,", Proc. SPIE vol 1088, Optical laser lithography II, march 1989, M.van den Brink, H,Jasper, S.Slonaker, P.van Wijnhoven, Frans Klaassen, "Step and Scan and Step and Repeat, a technology comparison" Proc. SPIE vol. 2726, Symposium on Micro lithography IX, march 1996

43 years overlay: 3 orders of magnitude down, Steppers[1]

2000: Multi-color alignment increased process robustness

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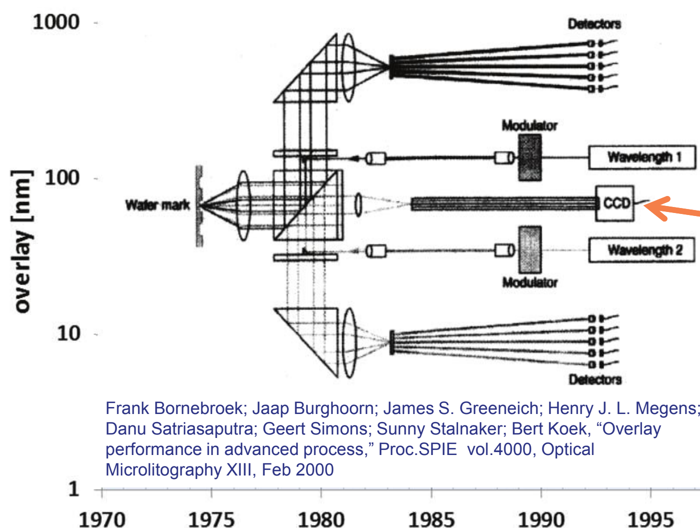

1000 100 10 1

overlay [nm]

system papers

application papers

Frank Bornebroek; Jaap Burghoorn; James S. Greeneich; Henry J. L. Megens; Danu Satriasaputra; Geert Simons; Sunny Stalnaker; Bert Koek, "Overlay performance in advanced process," Proc.SPIE vol.4000, Optical Microlitography XIII, Feb 2000

1970 1975 1980 1985 1990 1995 2000 2005 2010 2015 2020

[1]Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015

43 years overlay: 3 orders of magnitude down, Steppers[1]

2001: Increased metrology time at higher productivity using dual stage

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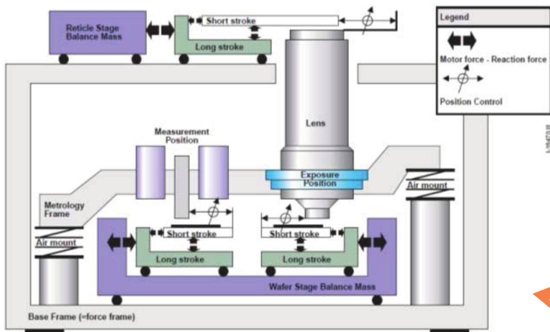
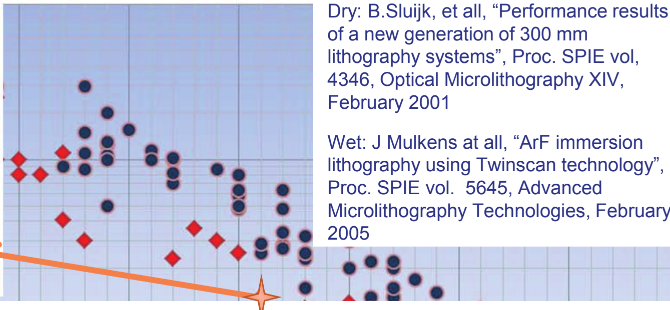
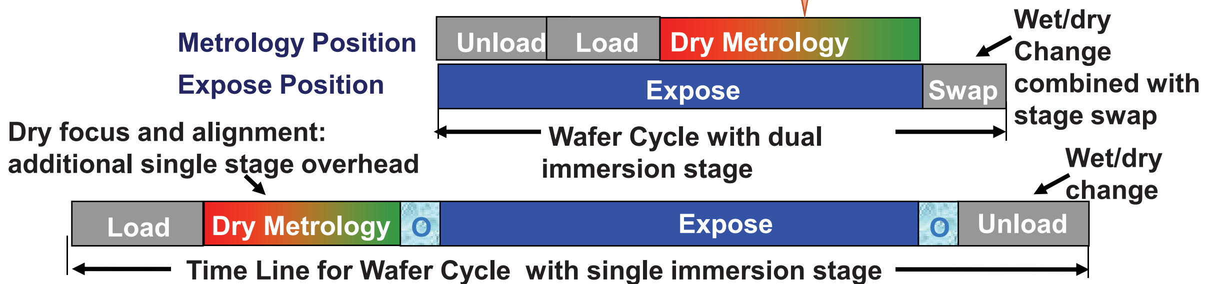




Dry: B.Sluijk, et all, "Performance results of a new generation of 300 mm lithography systems", Proc. SPIE vol, 4346, Optical Microlithography XIV, February 2001

Wet: J Mulkens at all, "ArF immersion lithography using Twinscan technology", Proc. SPIE vol. 5645, Advanced Microlithography Technologies, February 2005



43 years overlay: 3 orders of magnitude down, Steppers[1]

2007: Small process-compatible alignment markers by self-referencing

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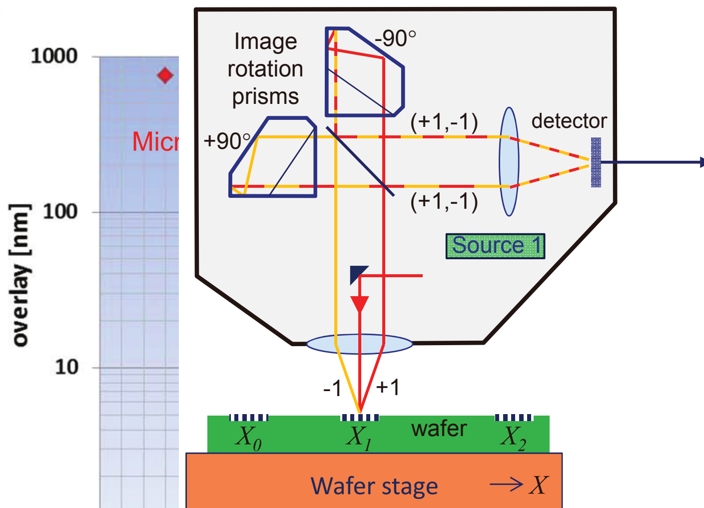

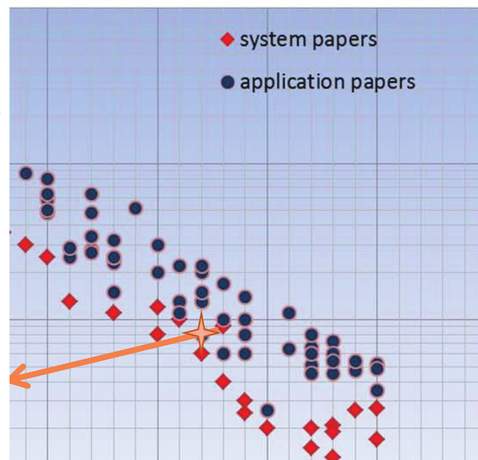

M. Miyasaki, H.Saito, T.Tamura, T.Uchiyama, P.Hinnen, H.W.Lee, M.van Kemenade, M.Shahrjerdy, R.van Leeuwen, "The application of SMASH alignment system for 65-55 nm logic devices. Proc. SPIE vol. 6518, Metrology, inspection and process control for microlithography XXI February 2007,
A den Boef, "Optical wafer metrology sensors for process-robust CD and overlay control in semiconductor device manufacturing" ,Surf. Topogr.: Metrol. Prop. 4 (2016) 023001

[1]Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015

43 years overlay: 3 orders of magnitude down, corrections[1]

User-definable correction capability increased ~4 orders of magnitude

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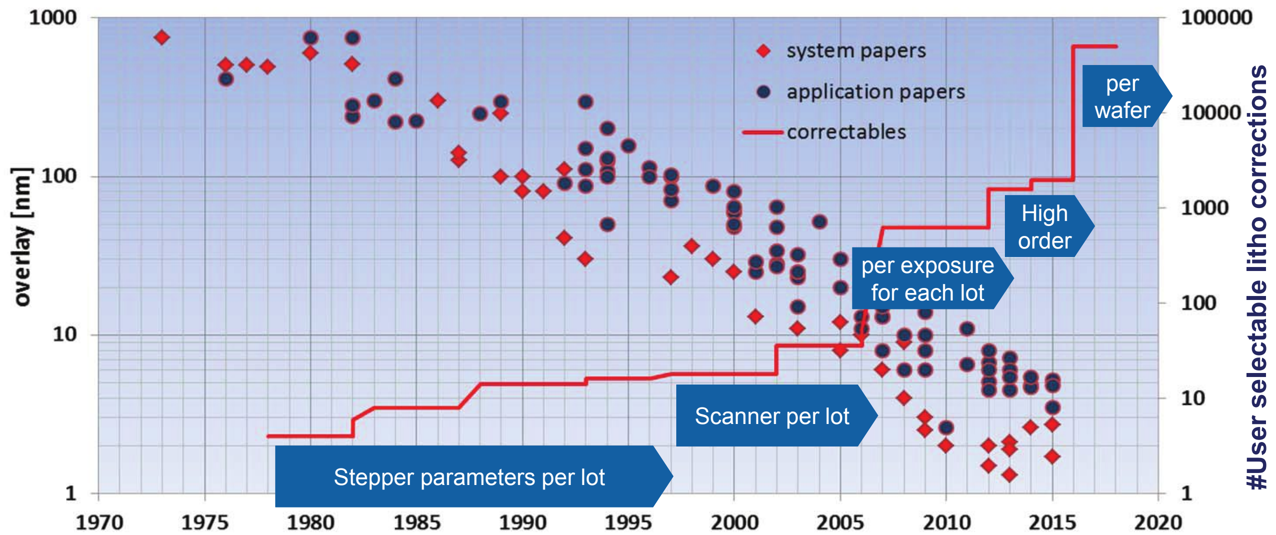

[1]Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015

43 years overlay: 3 orders of magnitude down, corrections

1979: Manual stepper setup using verniers on reduction steppers

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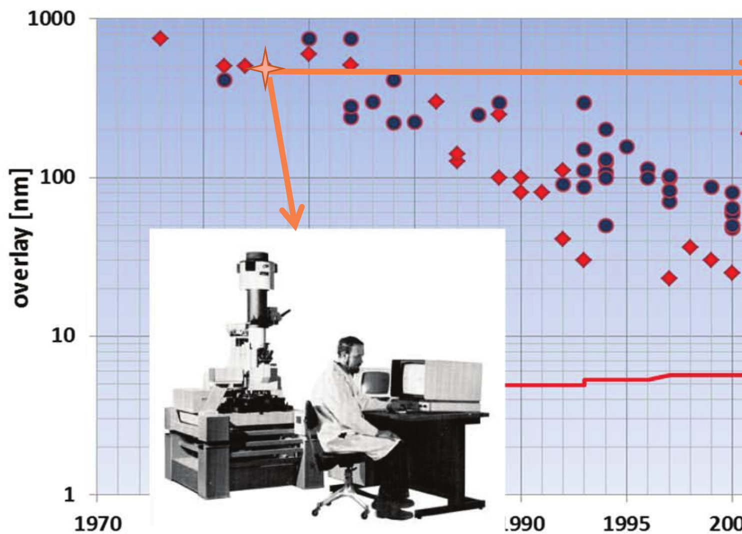

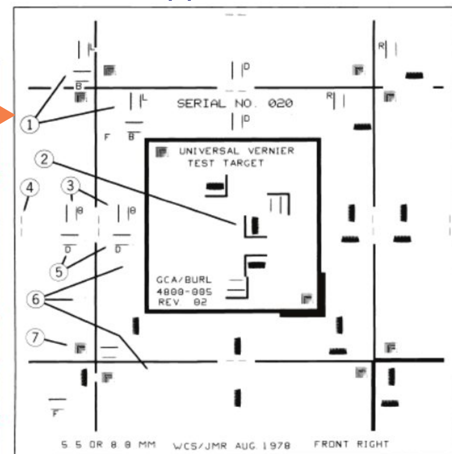

KEY: 1. REDUCTION VERNIERS (TYPICAL)
2. PRECISION / REGISTRATION VERNIERS
3. ROTATION VERNIERS (TYPICAL)
4. RETICLE ALIGNMENT MARKS (TYPICAL)
5. DISTORTION VERNIERS (TYPICAL)
6. WAFER ALIGNMENT KEYS (TYPICAL)
7. RESOLUTION TARGET (TYPICAL)

#User selectable litho corrections

William. C. Schneider, "Testing The Mann Type 4800DSW™ Wafer Stepper", Proc. SPIE vol. 0174, Developments in Semiconductor Microlithography IV, April, 1979

43 years overlay: 3 orders of magnitude down, corrections[1]

1982: 8-parameter stepper overlay setup model

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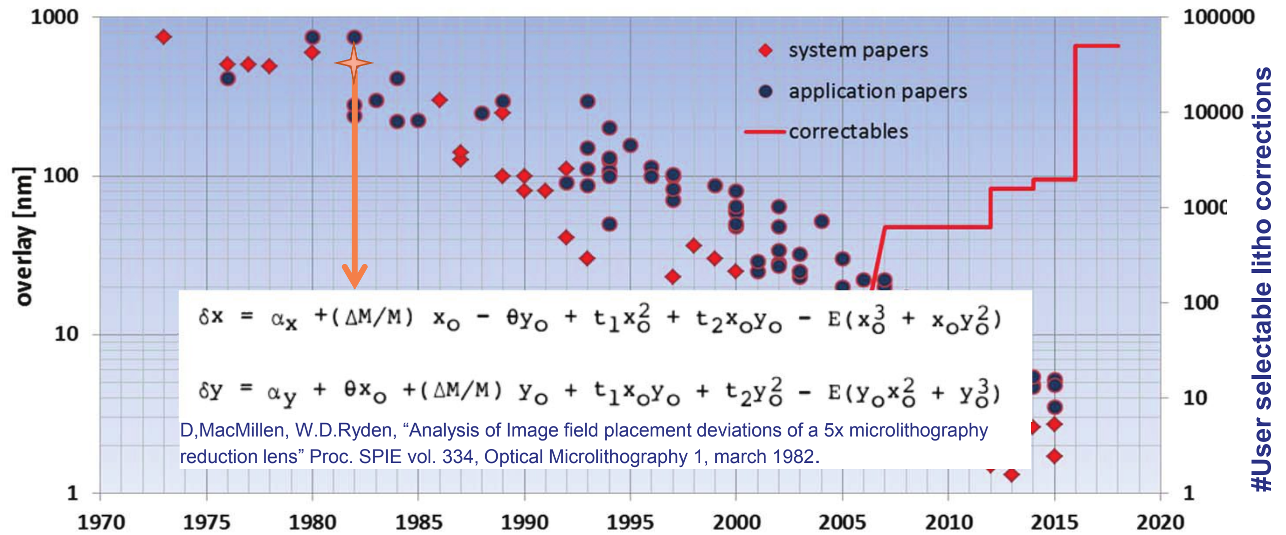

[1]Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015

43 years overlay: 3 orders of magnitude down, corrections

1988: 25-parameter automatic alignment setup

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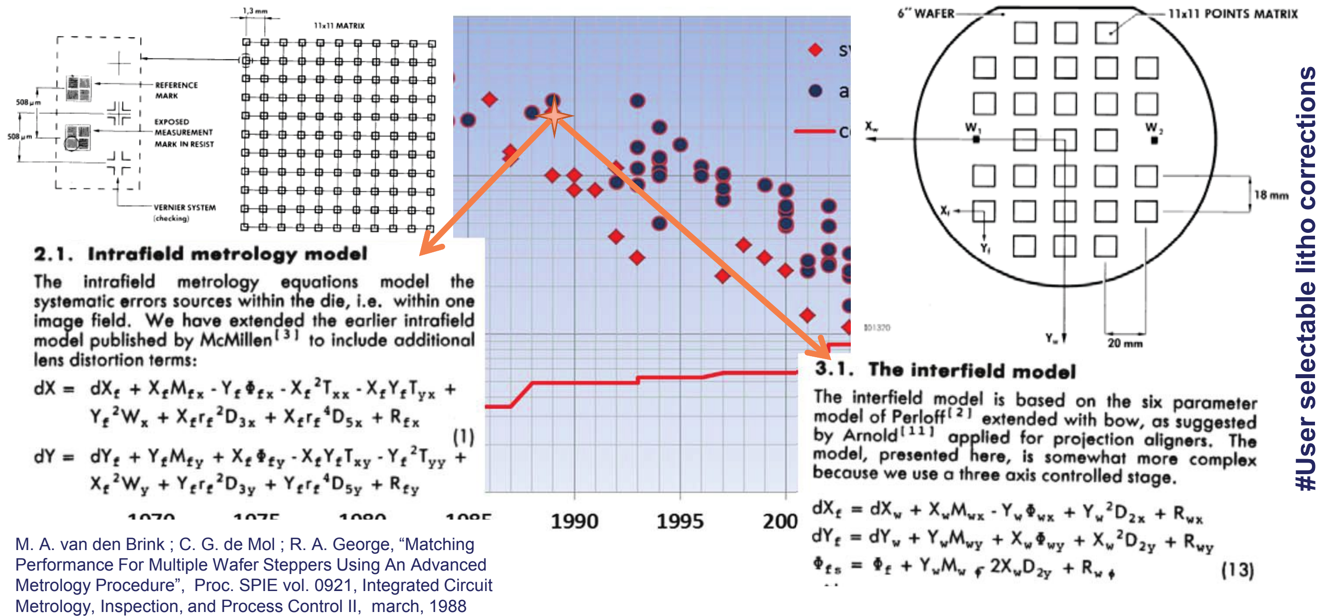

43 years overlay: 3 orders of magnitude down, corrections

1993: i-line to DUV automated 99-parameter 8-machine matching setup

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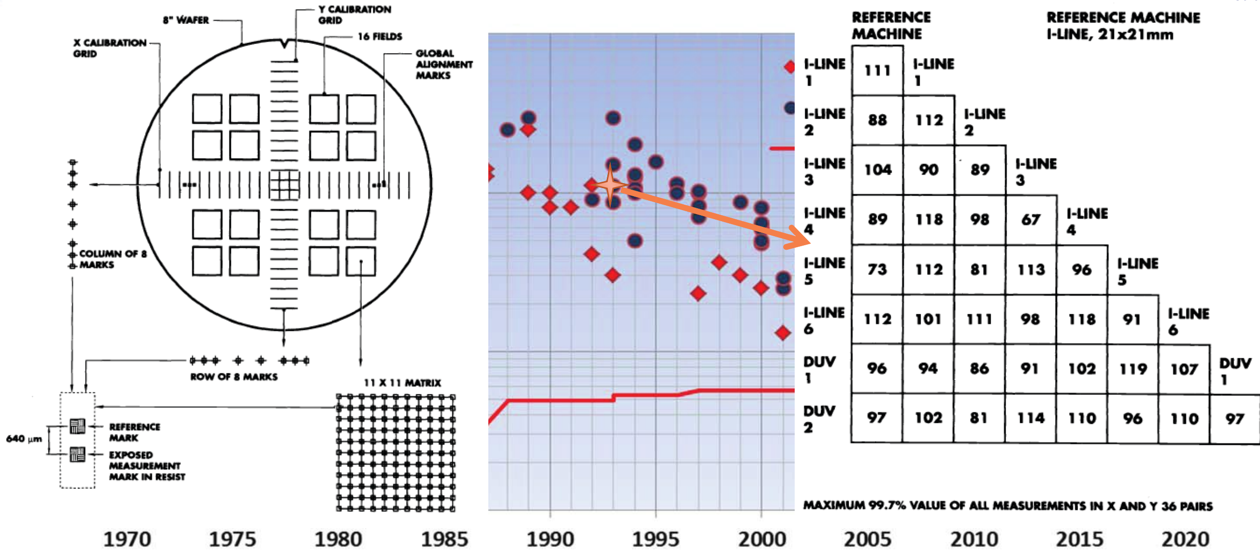

REFERENCE MACHINE		I-LINE 1	I-LINE 2	I-LINE 3	I-LINE 4	I-LINE 5	I-LINE 6	DUV 1
I-LINE 1	111							
I-LINE 2	88	112						
I-LINE 3	104	90	89					
I-LINE 4	89	118	98	67				
I-LINE 5	73	112	81	113	96			
I-LINE 6	112	101	111	98	118	91		
DUV 1	96	94	86	91	102	119	107	
DUV 2	97	102	81	114	110	96	110	97

Martin A. van den Brink; Chris G. M. de Mol; Judon M. D. Stoeldraijer ,"Matching of multiple-wafer steppers for 0.35-µm lithography using advanced optimization schemes", Proc. SPIE vol.1926, Integrated Circuit Metrology, Inspection, and Process Control VII, February, 1993

43 years overlay: 3 orders of magnitude down, corrections[1]

2007: 20-parameter higher-order user-definable corrections per field

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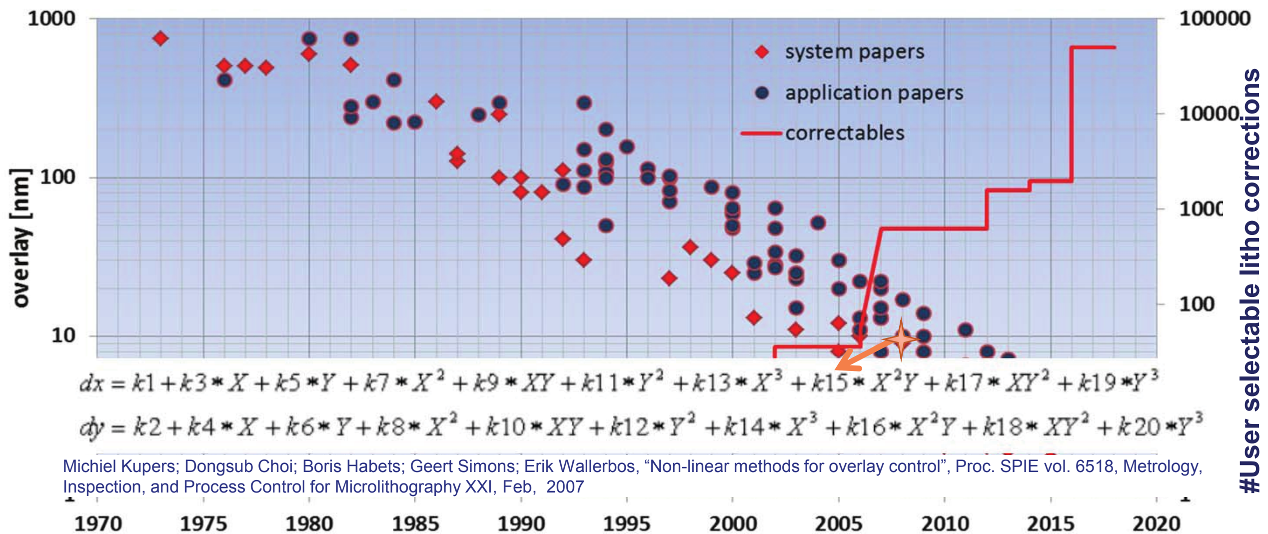
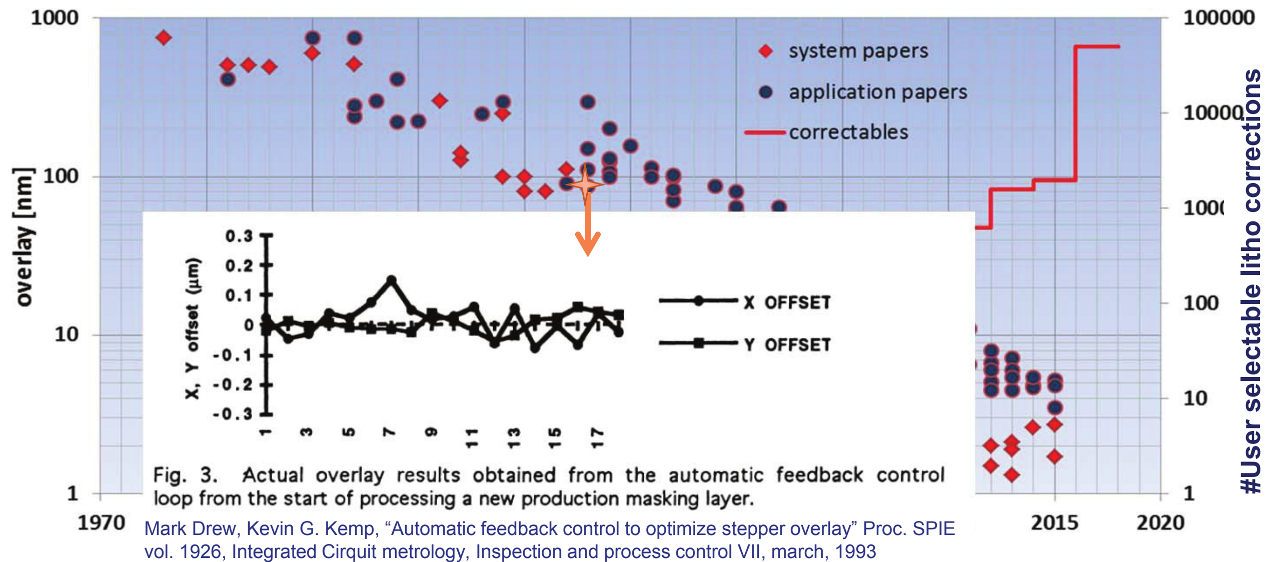


[1]Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015


43 years overlay: 3 orders of magnitude down, feedback¹
1993: Stepper external feedback control
ASML
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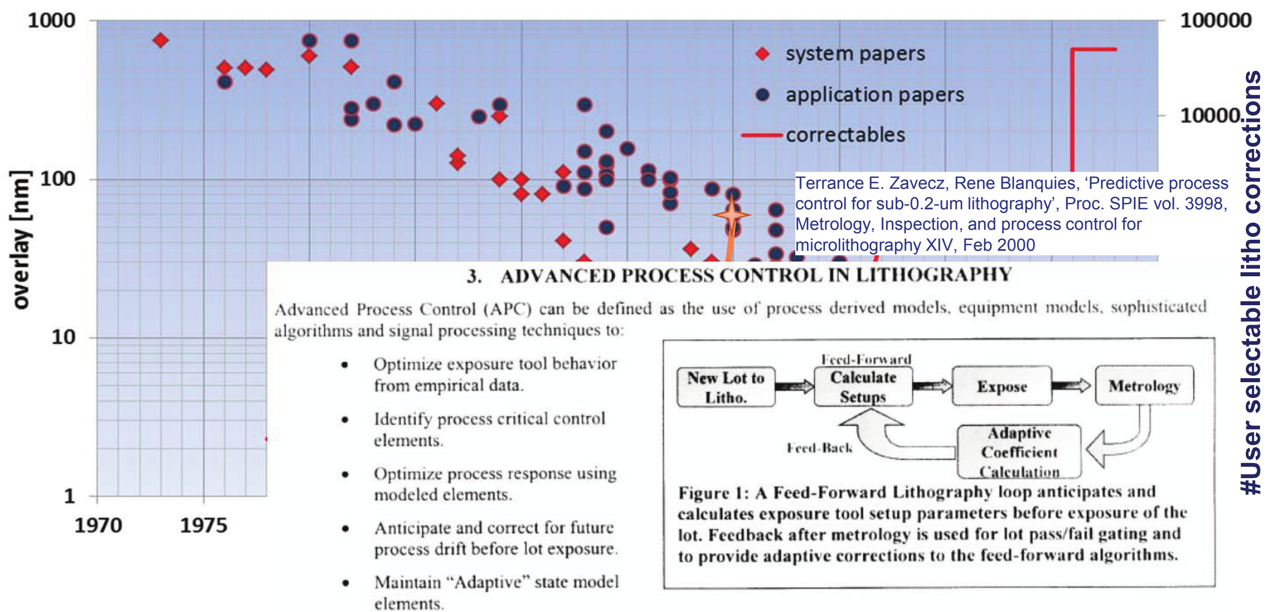
system papers
application papers
correctables
overlay [nm]
#User selectable litho corrections
X OFFSET
Y OFFSET
X, Y offset (µm)
Fig. 3. Actual overlay results obtained from the automatic feedback control loop from the start of processing a new production masking layer.
Mark Drew, Kevin G. Kemp, "Automatic feedback control to optimize stepper overlay" Proc. SPIE vol. 1926, Integrated Cirquit metrology, Inspection and process control VII, march, 1993
¹Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015


43 years overlay: 3 orders of magnitude down, feedback
2000: Stepper advanced process control
ASML
Public
Slide 20
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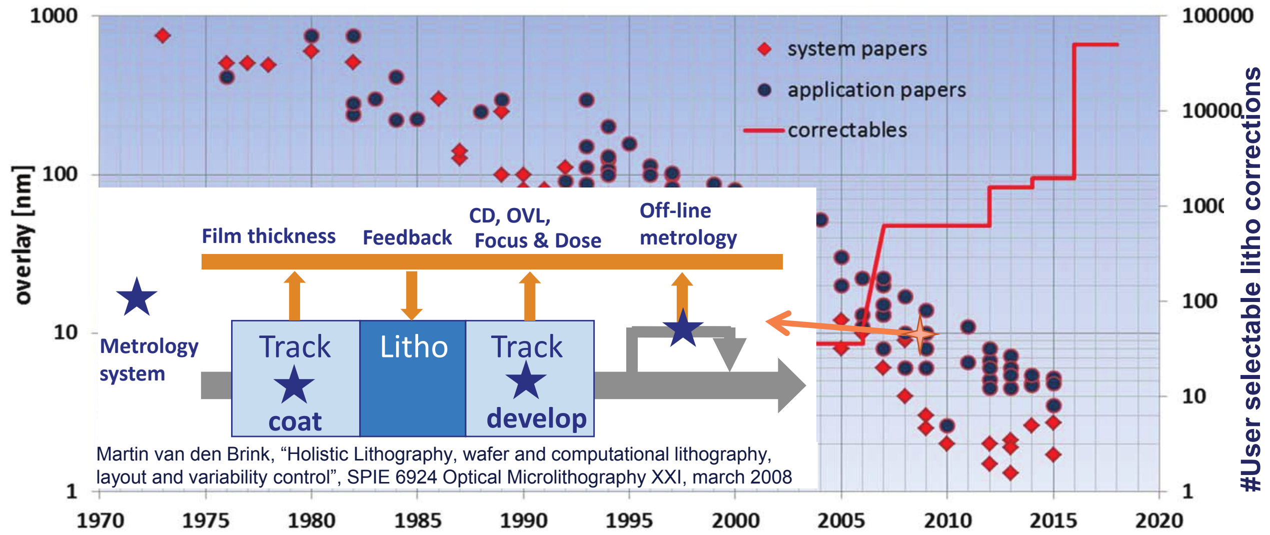
system papers
application papers
correctables
overlay [nm]
#User selectable litho corrections
Terrance E. Zavecz, Rene Blanquies, 'Predictive process control for sub-0.2-um lithography', Proc. SPIE vol. 3998, Metrology, Inspection, and process control for microlithography XIV, Feb 2000
3. ADVANCED PROCESS CONTROL IN LITHOGRAPHY
Advanced Process Control (APC) can be defined as the use of process derived models, equipment models, sophisticated algorithms and signal processing techniques to:
Optimize exposure tool behavior from empirical data.
Identify process critical control elements.
Optimize process response using modeled elements.
Anticipate and correct for future process drift before lot exposure.
Maintain "Adaptive" state model elements.
New Lot to Litho.
Feed-Forward
Calculate Setups
Expose
Metrology
Feed-Back
Adaptive Coefficient Calculation
Figure 1: A Feed-Forward Lithography loop anticipates and calculates exposure tool setup parameters before exposure of the lot. Feedback after metrology is used for lot pass/fail gating and to provide adaptive corrections to the feed-forward algorithms.


43 years overlay: 3 orders of magnitude down, feedback¹
2008: Litho feedforward and feedback control
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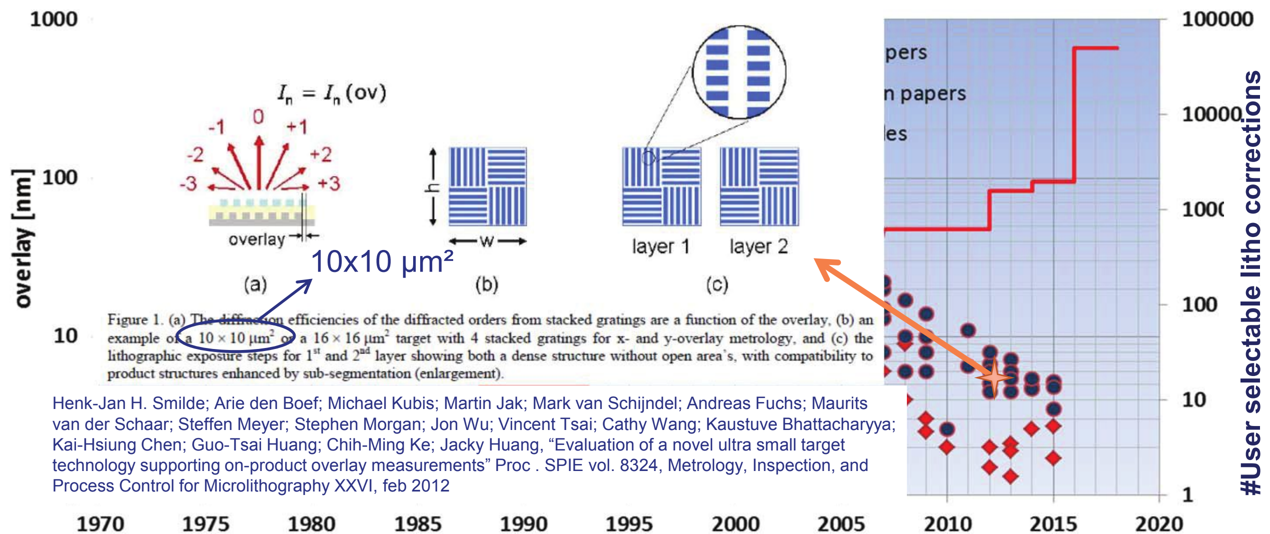
overlay [nm]
#User selectable litho corrections
system papers
application papers
correctables
Film thickness
Feedback
CD, OVL, Focus & Dose
Off-line metrology
Metrology system
Track coat
Litho
Track develop
Martin van den Brink, "Holistic Lithography, wafer and computational lithography, layout and variability control", SPIE 6924 Optical Microlithography XXI, march 2008
¹Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015


43 years overlay: 3 orders of magnitude down, feedback¹
2012: Small target design allowing on-product targets
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overlay [nm]
#User selectable litho corrections
$I_n = I_n(\mathrm{ov})$
overlay
10x10 µm²
layer 1
layer 2
(a)
(b)
(c)
Figure 1. (a) The diffraction efficiencies of the diffracted orders from stacked gratings are a function of the overlay, (b) an example of a 10 × 10 µm² or a 16 × 16 µm² target with 4 stacked gratings for x- and y-overlay metrology, and (c) the lithographic exposure steps for 1st and 2nd layer showing both a dense structure without open area's, with compatibility to product structures enhanced by sub-segmentation (enlargement).
Henk-Jan H. Smilde; Arie den Boef; Michael Kubis; Martin Jak; Mark van Schijndel; Andreas Fuchs; Maurits van der Schaar; Steffen Meyer; Stephen Morgan; Jon Wu; Vincent Tsai; Cathy Wang; Kaustuve Bhattacharyya; Kai-Hsiung Chen; Guo-Tsai Huang; Chih-Ming Ke; Jacky Huang, "Evaluation of a novel ultra small target technology supporting on-product overlay measurements" Proc . SPIE vol. 8324, Metrology, Inspection, and Process Control for Microlithography XXVI, feb 2012
¹Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015

43 years overlay: 3 orders of magnitude down[1]

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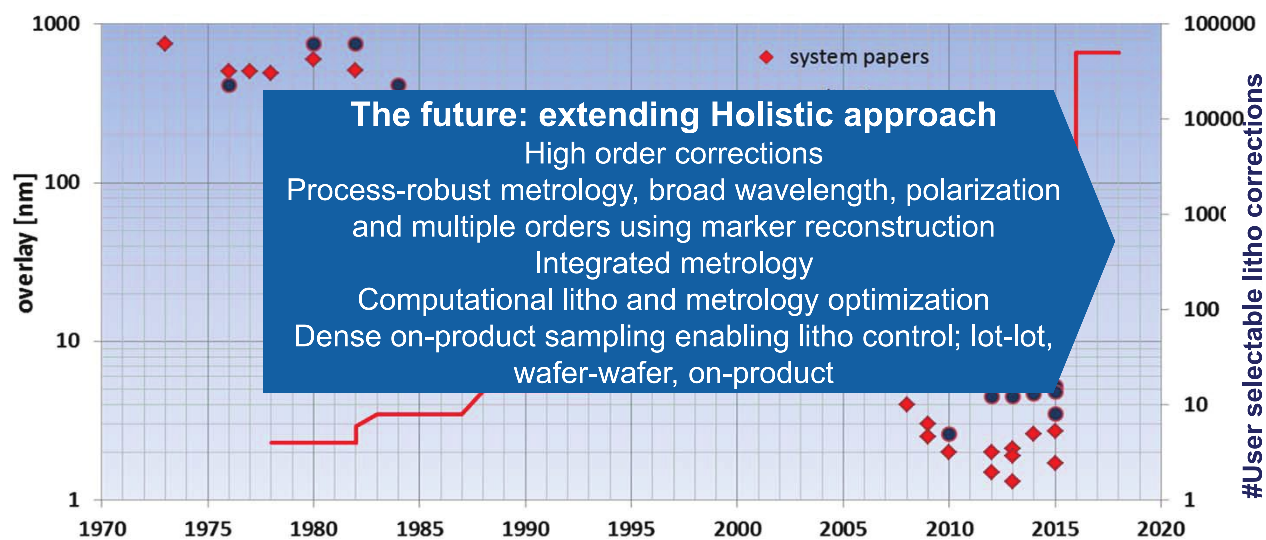

[1]Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015

Content

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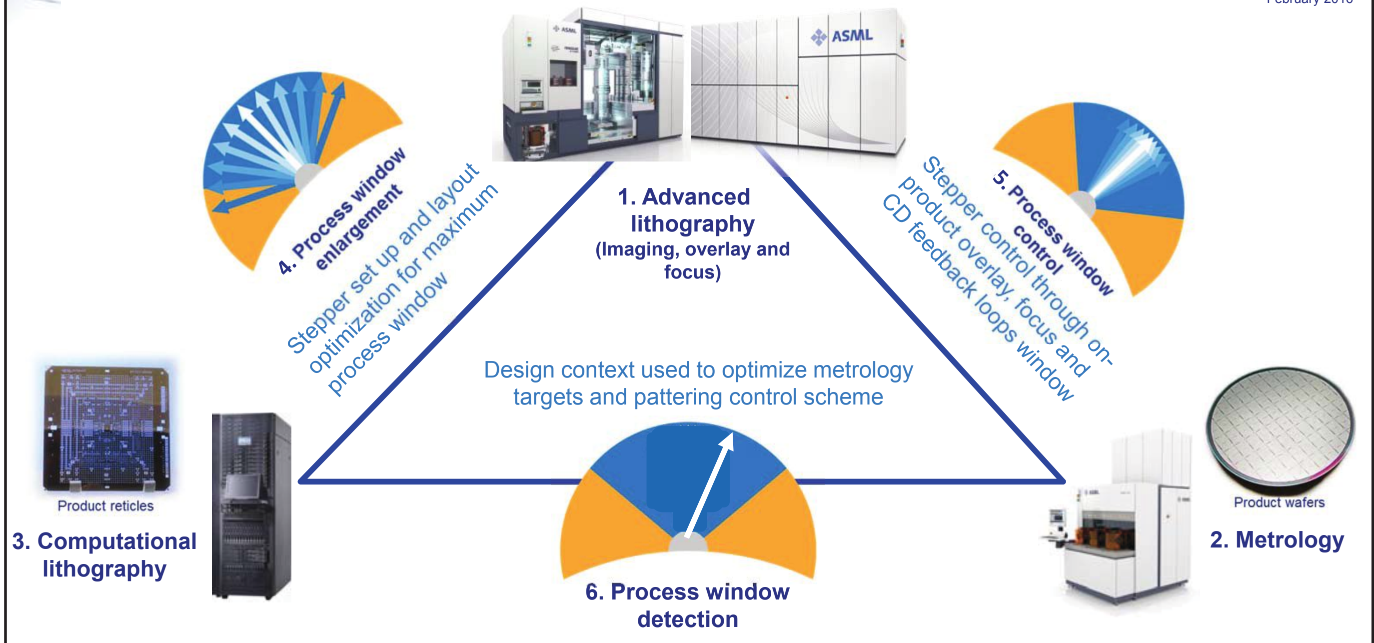
- 43 years overlay metrology in microlithography: How did we get here?
- Holistic Lithography: where we are today
- The future of Holistic lithography: where we are going
- Summary


ASML holistic lithography: 6 competences
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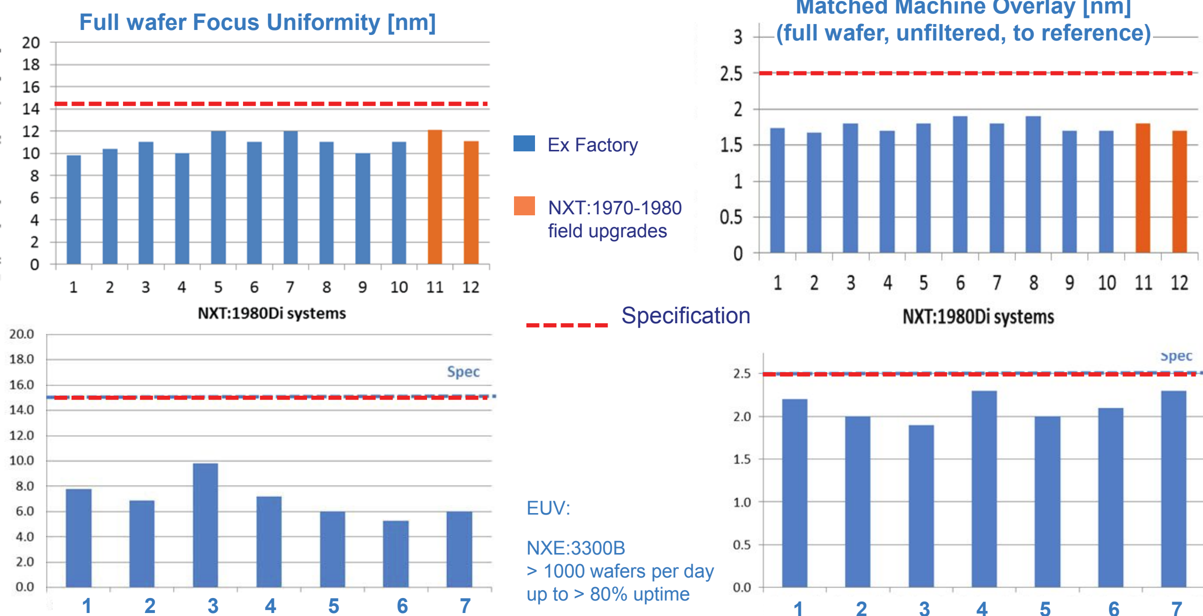
1. Advanced lithography
(Imaging, overlay and focus)
4. Process window enlargement
Stepper set up and layout optimization for maximum process window
5. Process window control
Stepper control through on-product overlay, focus and CD feedback loops window
Design context used to optimize metrology targets and pattering control scheme
Product reticles
3. Computational lithography
Product wafers
2. Metrology
6. Process window detection


1) Advanced Lithography: significantly improved
on critical parameters both for immersion as well EUV
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Full wafer Focus Uniformity [nm]
NXT:1980Di systems
Matched Machine Overlay [nm]
(full wafer, unfiltered, to reference)
NXT:1980Di systems
Ex Factory
NXT:1970-1980
field upgrades
Specification
Spec
EUV:
NXE:3300B
> 1000 wafers per day
up to > 80% uptime

2) Metrology: boosts performance and productivity

Increase metrology accuracy, cut cost of metrology by a factor of 4

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Sensor
- New sensor architecture optimized for dedicated High NA µDBO/F detection branch
- Higher µDBO/F magnification
- Parallel 1st order wedge acquisition allowing for High performance / high throughput mode

Illumination
- Increased source power
- Extension to higher wavelength
- Variable spot size selection

		YieldStar 250	YieldStar 350
Application	Detection NA	0.4 NA 2 acquisitions +1 order and -1 order	0.9 NA 1 acquisition +1 order and -1 order
	Wavelength	425 – 780nm	425 – 885nm
Productivity	Spot size	25µm Spot size 3-Layer OVL	37µm Spot size 6-Layer OVL
	Measurement time	0.35s	0.2s
	Maximum sampling	3000pts / lot	12000pts / lot

3) Computational Lithography: Robust modeling capability

Negative Tone Development (NTD) resist with physical modeling accuracy improved 59%

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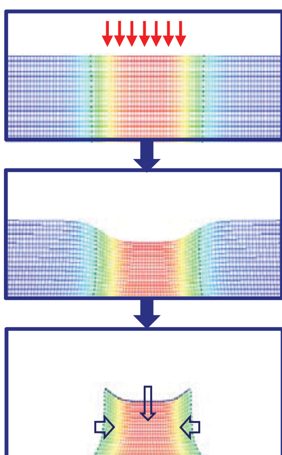
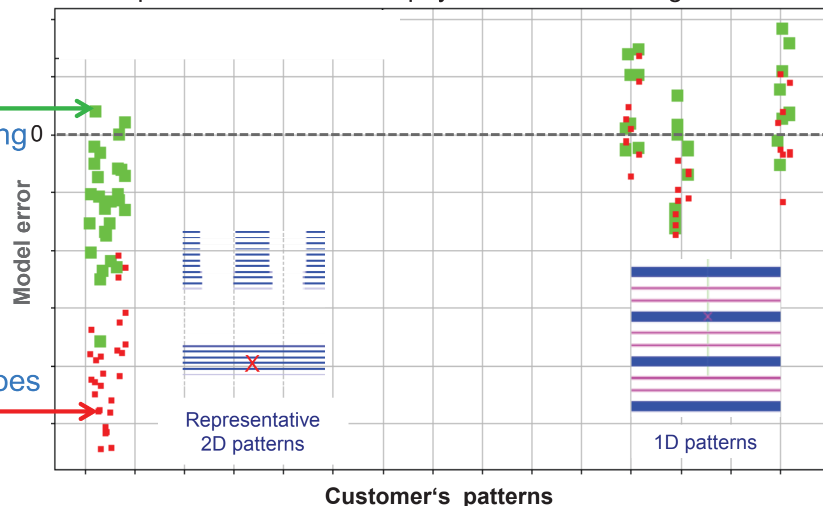


Physical NTD resist model accounts for 3 dimensional shrink impacting 2D OPC accuracy

Empirical NTD resist model does not capture 3 dimensional shrink impact

Model error (simulated CD – wafer CD) comparison between empirical NTD model and physical resist shrinkage model



4) Process Window Enhancement: EUV optimization

over an increasingly large parameter space improves window 27%

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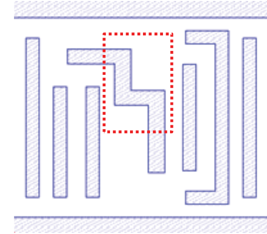
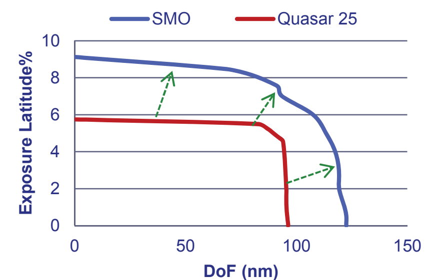
Illumination Pupil		CDU (nm)	Pattern placement error (nm)	2x Line Edge Roughness (nm)	Total EPE (nm)	Simulated contour
POR Quasar 25		1.4	1.0	3.9	4.3	
		-21%	-20%	-13%	-14%	
SMO		1.1	0.8	3.4	3.7	

Total EPE = $((CDU)^2 + (PPE)^2 + (2xLER)^2)^{1/2}$

EPE: Edge Placement Error determined by combination of CD, pattern placement and Line Edge Roughness



27% improvement in total process window based on all 3 metrics: CDU, pattern placement and LER.



5) Metrology: >30% improved wafer edge overlay

on Memory process stack using integrated and diffraction-based overlay metrology, fingerprint capturing and sampling optimization

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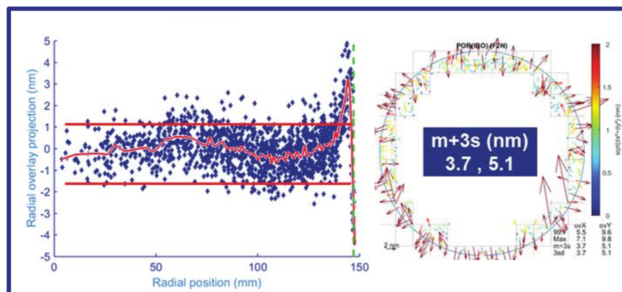
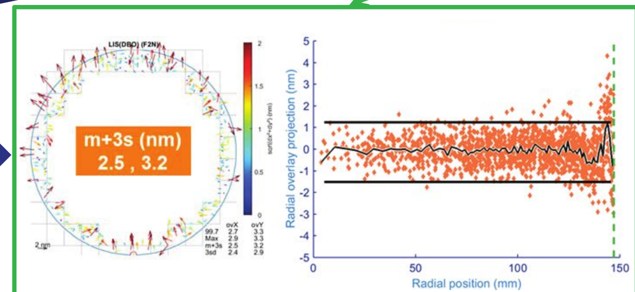
	Full wafer X / Y Overlay (m+3σ)		Wafer Edge X / Y Overlay (m+3σ)	
Control mode	**Stand Alone Image Based Overlay standard sampling**	**Stand Alone/ Integrated Diffraction Based Overlay & sampling optimization**	**Stand Alone Image Based Overlay standard sampling**	**Stand Alone/ Integrated Diffraction Based Overlay & sampling optimization**
Layer A	**2.7 / 4.5**	**2.7 / 2.9 (IM)**	**3.2 / 3.6**	**3.2 / 3.5 (IM)**
Layer B	**3.6 / 4.6**	**2.9 / 4.1 (SA)**	**3.7 / 5.1**	**2.5 / 3.2 (SA)**



>30%



6) Process Window Detection: Engineering efficiency improvement by computational assisted alignment marker, recipe and sampling scheme optimization

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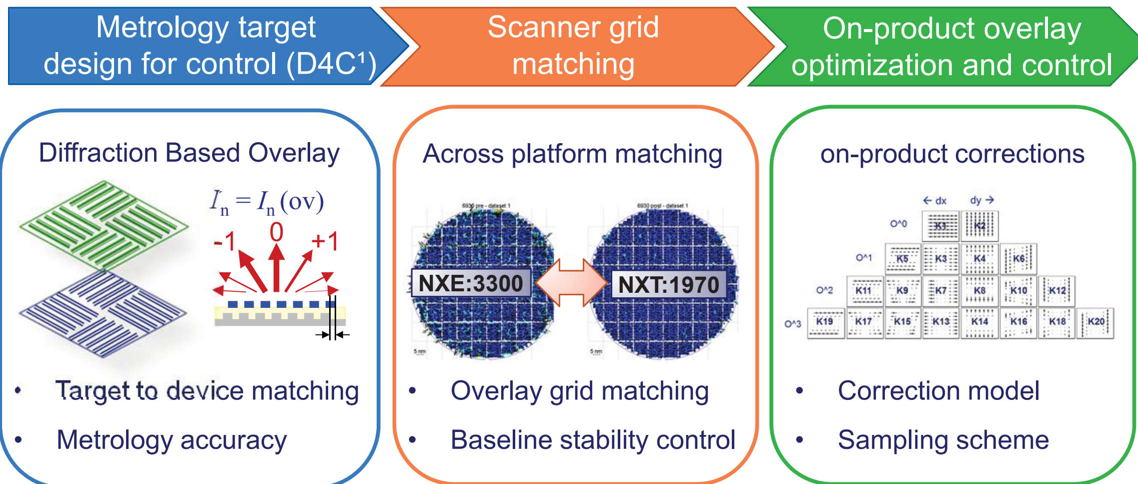

[1]YS Kim, Y.S.hwang, M.R.Jung, J. H. Yoo, W.T.Kwon, K.Ryan, P.Tuffy, Y. Zhang, S.Park , N.L.Oh, C.Park . M.Shahrjerdy, R Werkam, K.T.Sun, J.M.Buyn,"Improving full-wafer on-product overlay using computationally designed process robust and device-like metrology targets" Proc SPIE proc. 9424, Metrology, Inspection, and Process Control for Microlithography XXIX, Feb 2015

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- 43 years overlay metrology in microlithography: How did we get here?
- Holistic Lithography: where we are today
- The future of Holistic lithography: where we are going
  - Fingerprint estimation and Sampling optimization
  - Target design and recipe optimization
  - Pattern fidelity
- Summary

Challenges by balancing sampling and correction density
Improved noise suppression by determining fingerprint capture

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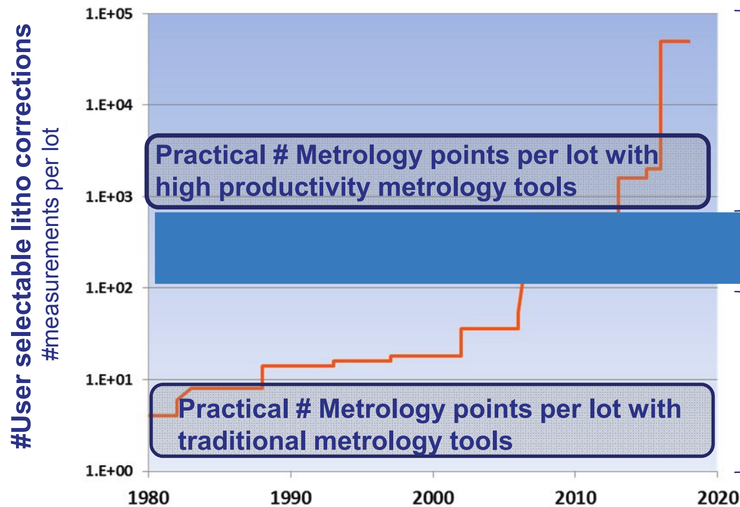

- Number of litho-compatible parameters is close to or exceeds number of measurements

→ Issue with noise suppression

- Typical number of parameters sufficient to capture fingerprint

→ Optimal noise reduction/fingerprint capture balance

- Not enough parameters for high-resolution litho-compatible fingerprint

→ Issue with fingerprint capture

Fingerprint capturing will improve correction noise

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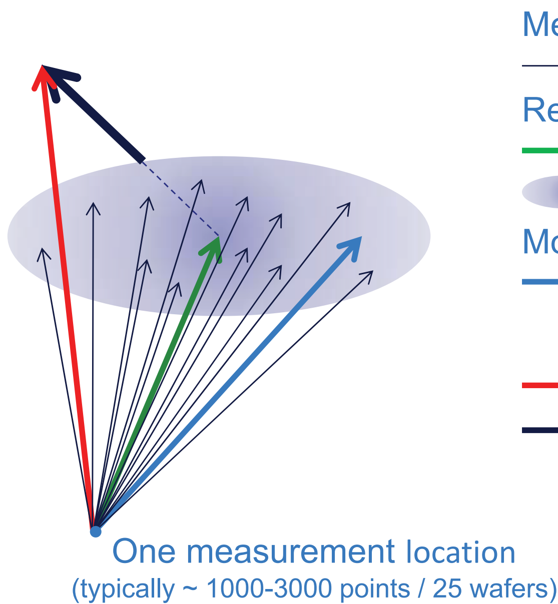

Measured
Overlay per wafer

Reference
Average overlay on this location
Statistical precision

Modeled fit results
Good model at this location:
Fit is within precision of reference

Not-so-good model: outside precision
Difference to edge of statistical precision:
non-captured fingerprint

Non-captured fingerprint = 0
if model fit is within precision

Fingerprint modeling can decrease # parameters >10x

resulting in better capturing the errors and reducing noise

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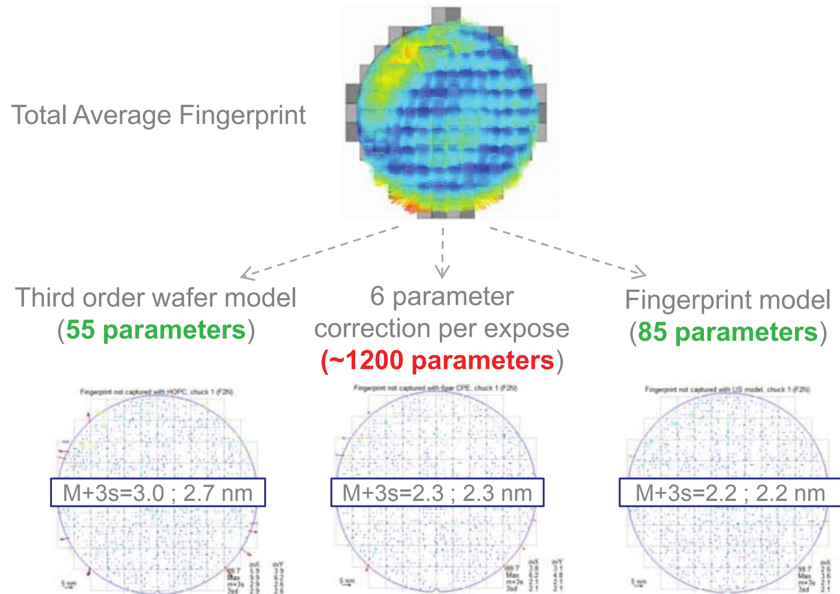

Errors not captured by the model

Reducing overlay by 25% and improving edge yield

Using an optimized sampling scheme

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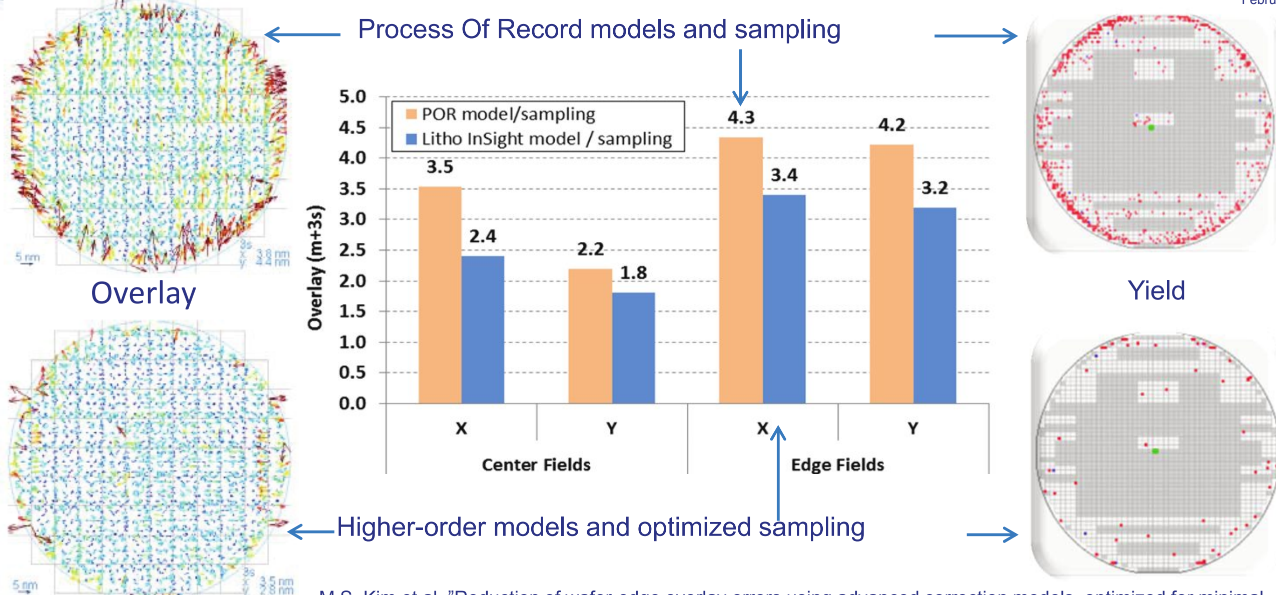

M.S. Kim et.al.,"Reduction of wafer-edge overlay errors using advanced correction models, optimized for minimal metrology requirements", SPIE Conference 9780-9 , February 2016

Content

- 43 years overlay metrology in microlithography, how did we get here
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  - Sampling optimization
  - Target design and recipe optimization
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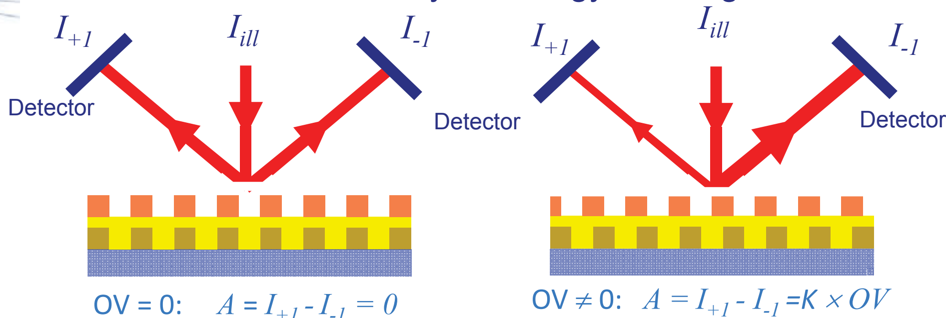
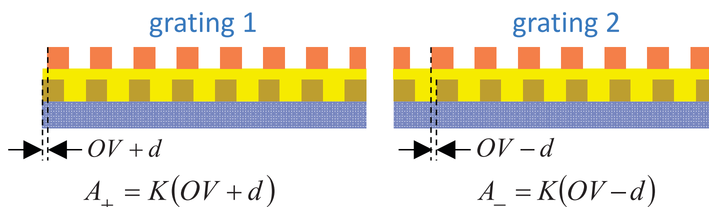
Diffraction-based process-robust overlay metrology

Fast and affordable overlay metrology allowing dense wafer sampling



OV = 0: $A = I_{+1} - I_{-1} = 0$ OV ≠ 0: $A = I_{+1} - I_{-1} = K \times OV$

Process-dependent K factor can be eliminated with 2 "biased" gratings:



$A_+ = K(OV + d)$ $A_- = K(OV - d)$

$$OV = d \frac{A_+ + A_-}{A_+ - A_-}$$

Accurately determined by mask writer

Accurately measured by YieldStar

A den Boef, "Optical wafer metrology sensors for process-robust CD and overlay control in semiconductor device manufacturing" ,Surf. Topogr.: Metrol. Prop. 4 (2016) 023001

Metrology target and recipe design requires optimization

to meet tight overlay requirements, computational approach needed to reduce the experimental verification/engineering time

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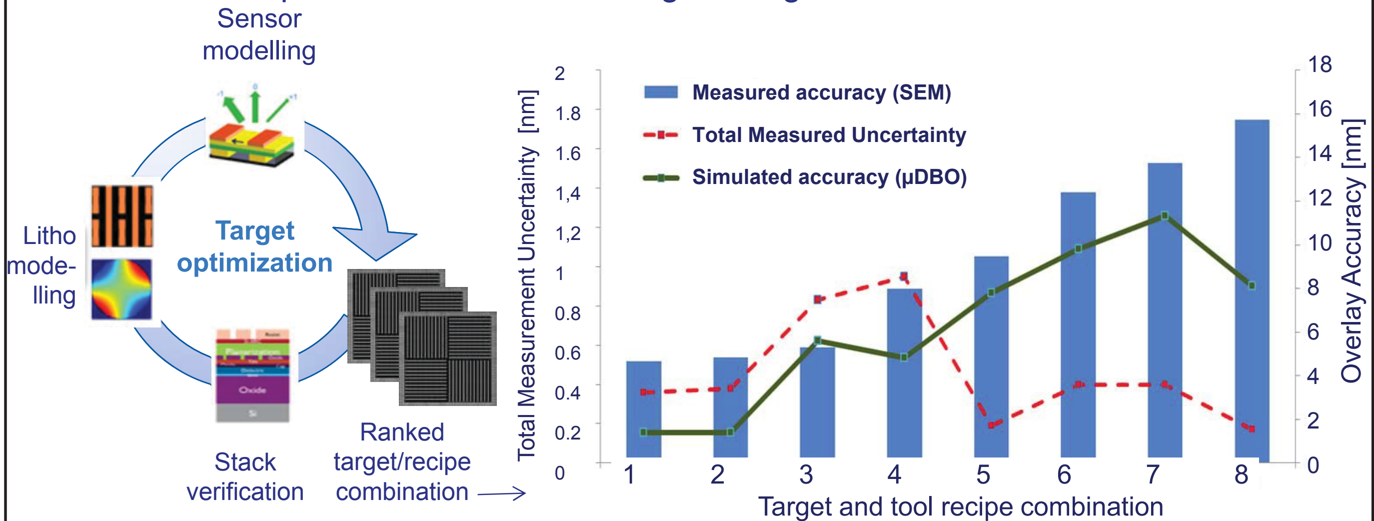

[1]YS Kim, Y.S.hwang, M.R.Jung, J. H. Yoo, W.T.Kwon, K.Ryan, P.Tuffy, Y. Zhang, S.Park , N.L.Oh, C.Park . M.Shahrjerdy, R Werkam, K.T.Sun, J.M.Buyn,"Improving full-wafer on-product overlay using computationally designed process robust and device-like metrology targets" Proc SPIE proc. 9424, Metrology, Inspection, and Process Control for Microlithography XXIX, Feb 2015

Using multi-wavelength to improve process robustness

on Yieldstar, reducing the influence of process asymmetry on overlay

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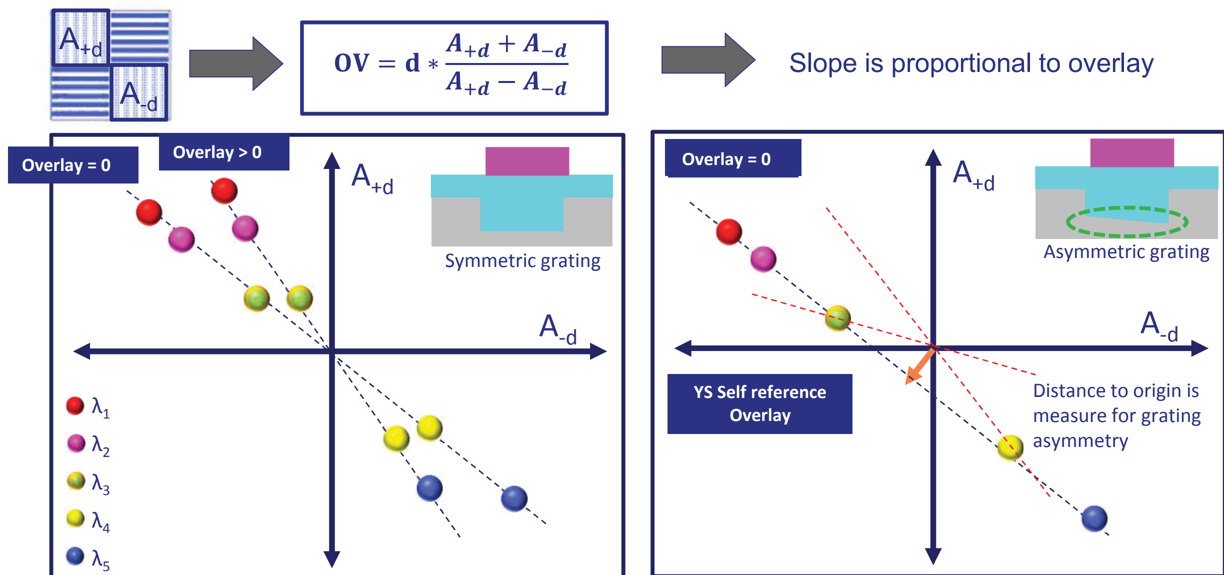

Leon Verstappen et.al., "Holistic Overlay Control for Multi-patterning Process layers at the 10-nm and 7-nm nodes", SPIE conference 9778-141, Feb 2016

Holistic Metrology Qualification selects recipe

with best overlay accuracy

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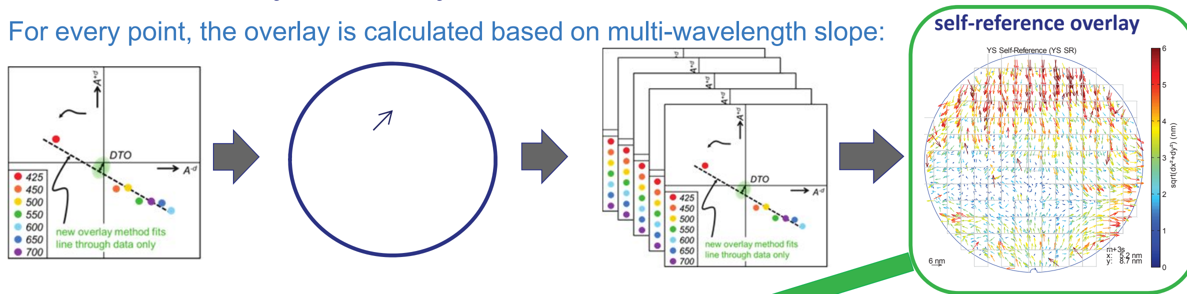
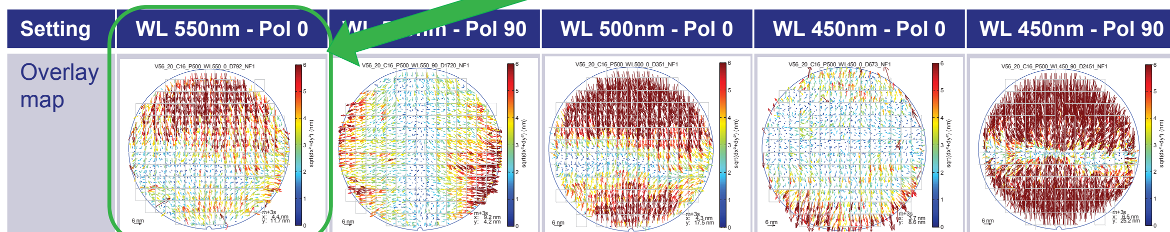
For every point, the overlay is calculated based on multi-wavelength slope:



The overlay maps of individual YS recipes are compared to the self-reference overlay:

Setting	WL 550nm - Pol 0	WL [illegible] - Pol 90	WL 500nm - Pol 0	WL 450nm - Pol 0	WL 450nm - Pol 90
Overlay map					



Leon Verstappen et.al., "Holistic Overlay Control for Multi-patterning Process layers at the 10-nm and 7-nm nodes", SPIE conference 9778-141, February 2016

Target to Device overlay mismatch reduced to < 0.9 nm

By optimizing target layout compatibility with device layout

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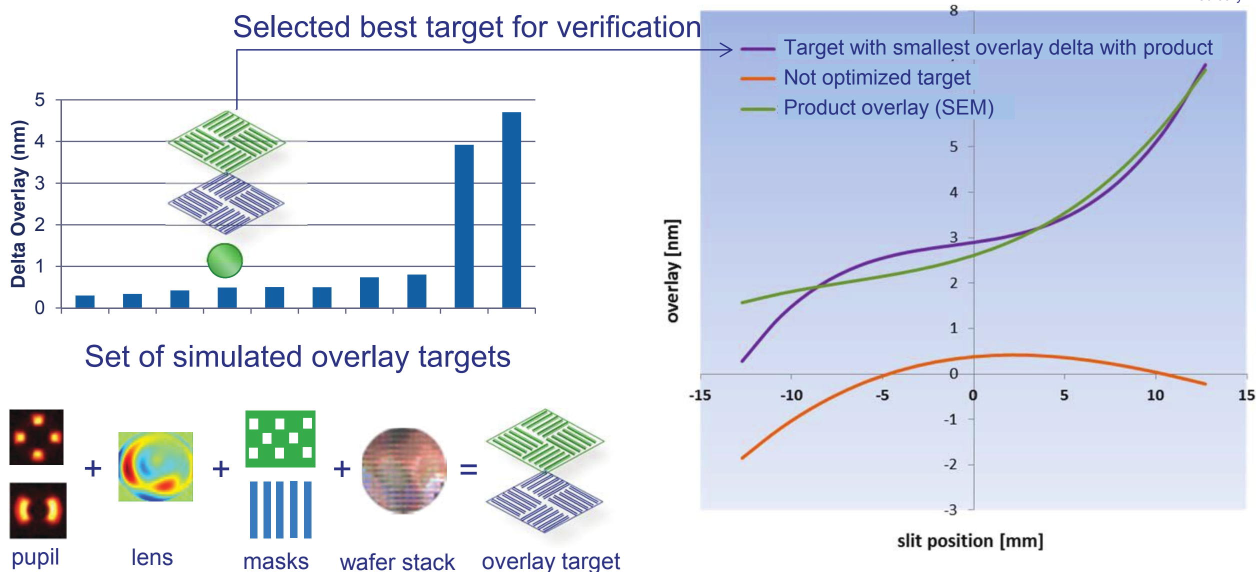

J.Zhou, "Eliminating the offset between overlay metrology and device pattern using computational target design" SPIE conference 9778-50, February 2016

Substantial alignment process robustness improvement

Using multiple wavelengths and polarizations in computational overlay simulation

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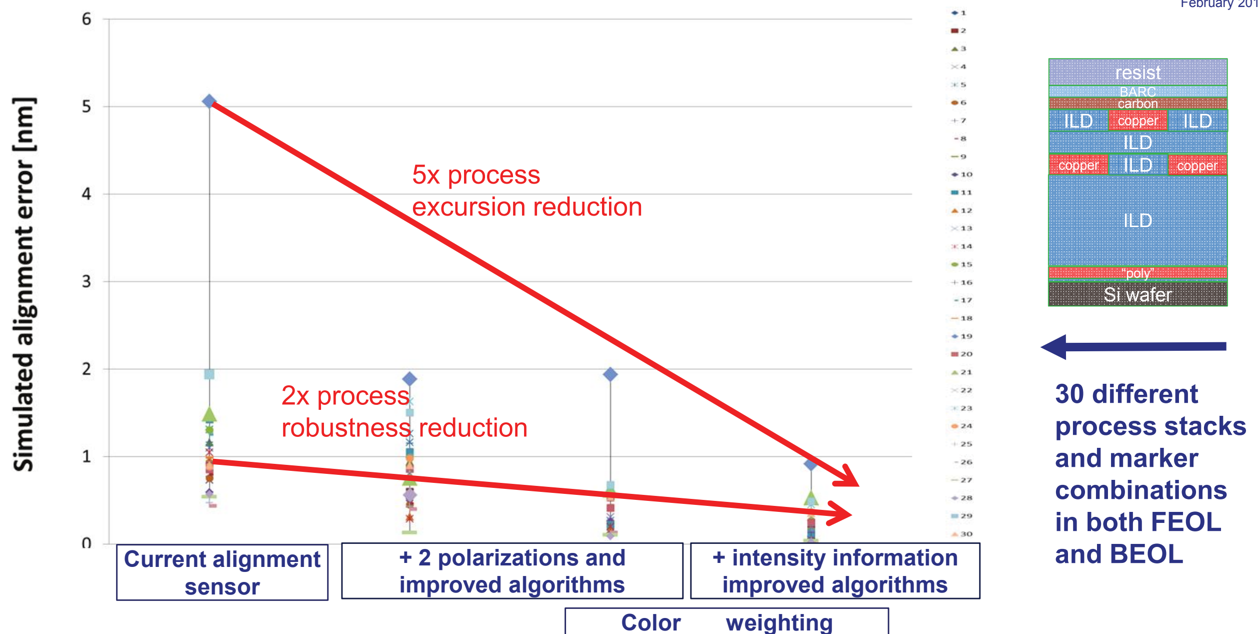

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- 43 years overlay metrology in microlithography: How did we get here?
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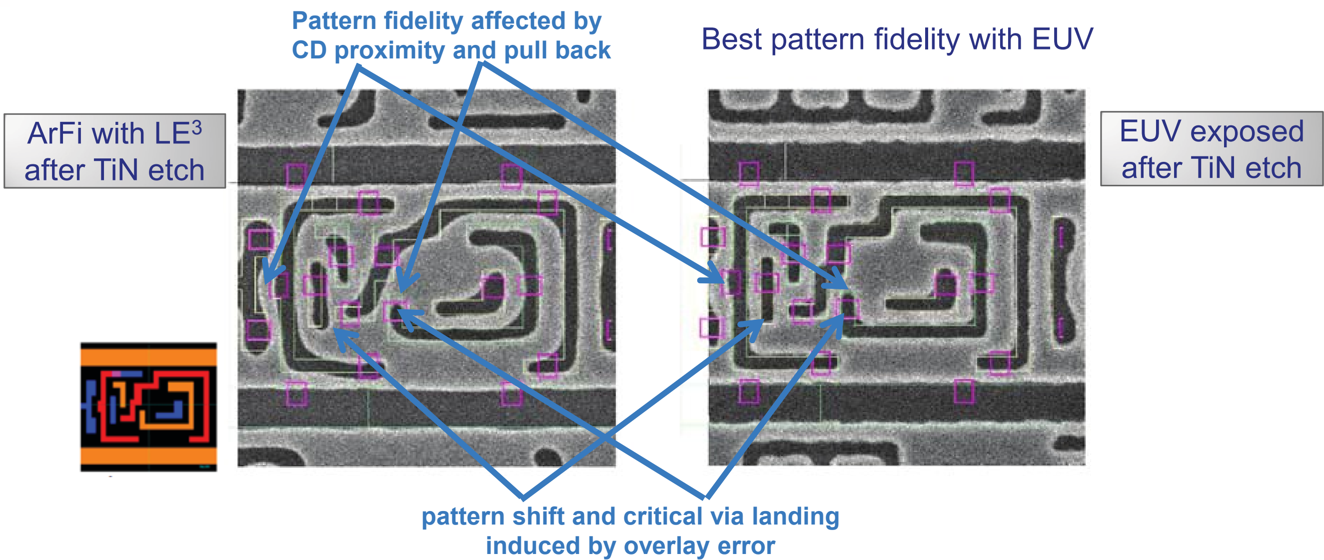
Pattern fidelity is impacted by multi-patterning and variability
Edge placement error affected by overlay and CD variations
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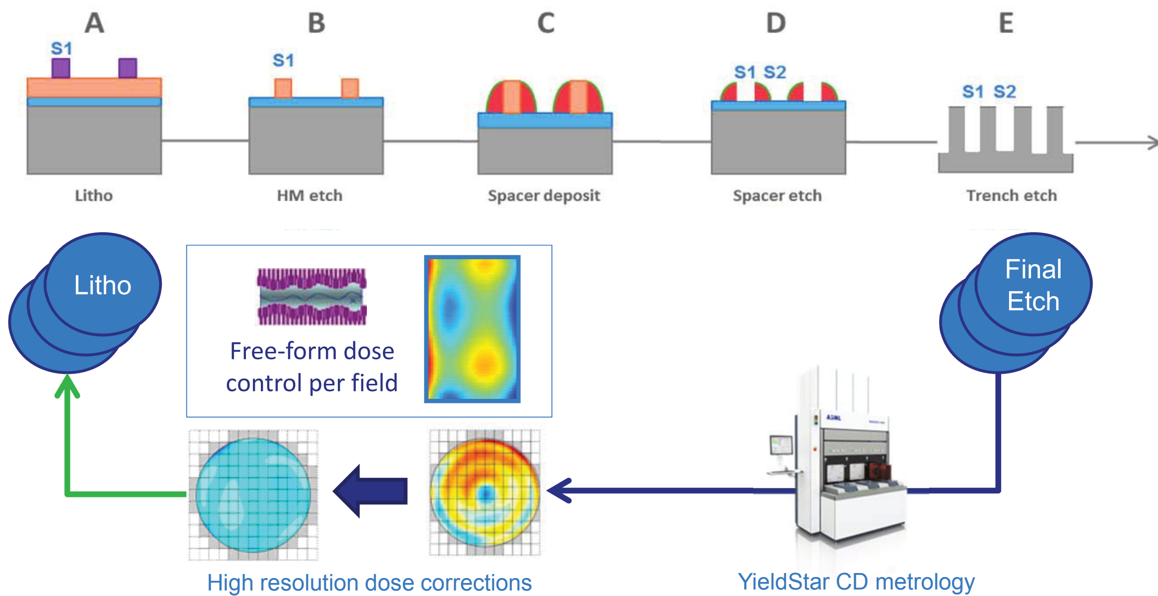
Pattern fidelity affected by
CD proximity and pull back
Best pattern fidelity with EUV
ArFi with LE3
after TiN etch
EUV exposed
after TiN etch
pattern shift and critical via landing
induced by overlay error
Data courtesy IMEC 10-nm logic design (M1)


CD variation after etch effectively controlled with scanner
Self-aligned double patterning fidelity optimized by balancing spacers S1 and S2
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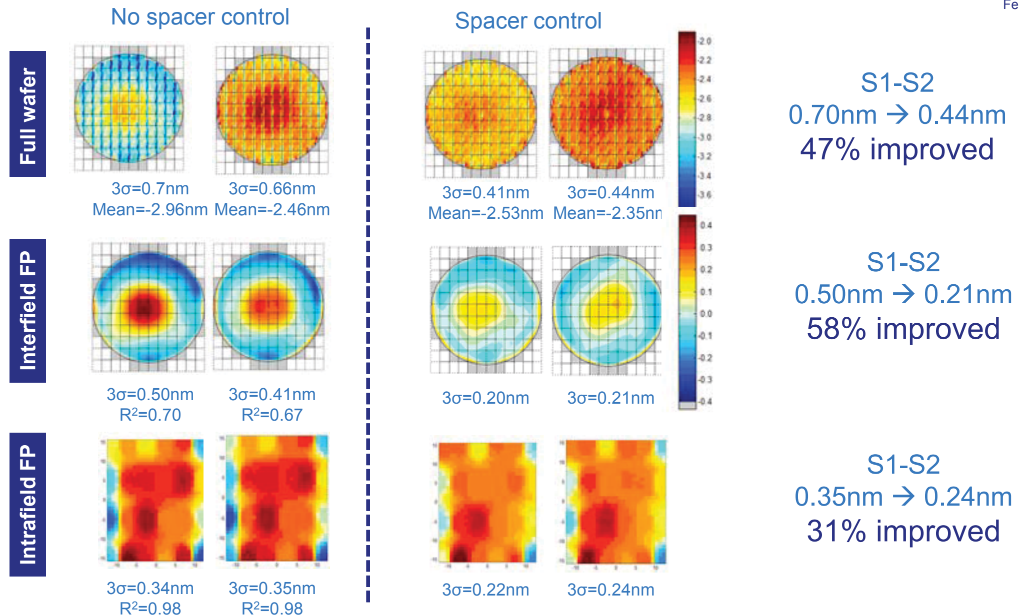
A
B
C
D
E
S1
S1
S1 S2
S1 S2
Litho
HM etch
Spacer deposit
Spacer etch
Trench etch
Litho
Free-form dose
control per field
Final
Etch
High resolution dose corrections
YieldStar CD metrology


CD fidelity improved by 2x using higher-order corrections
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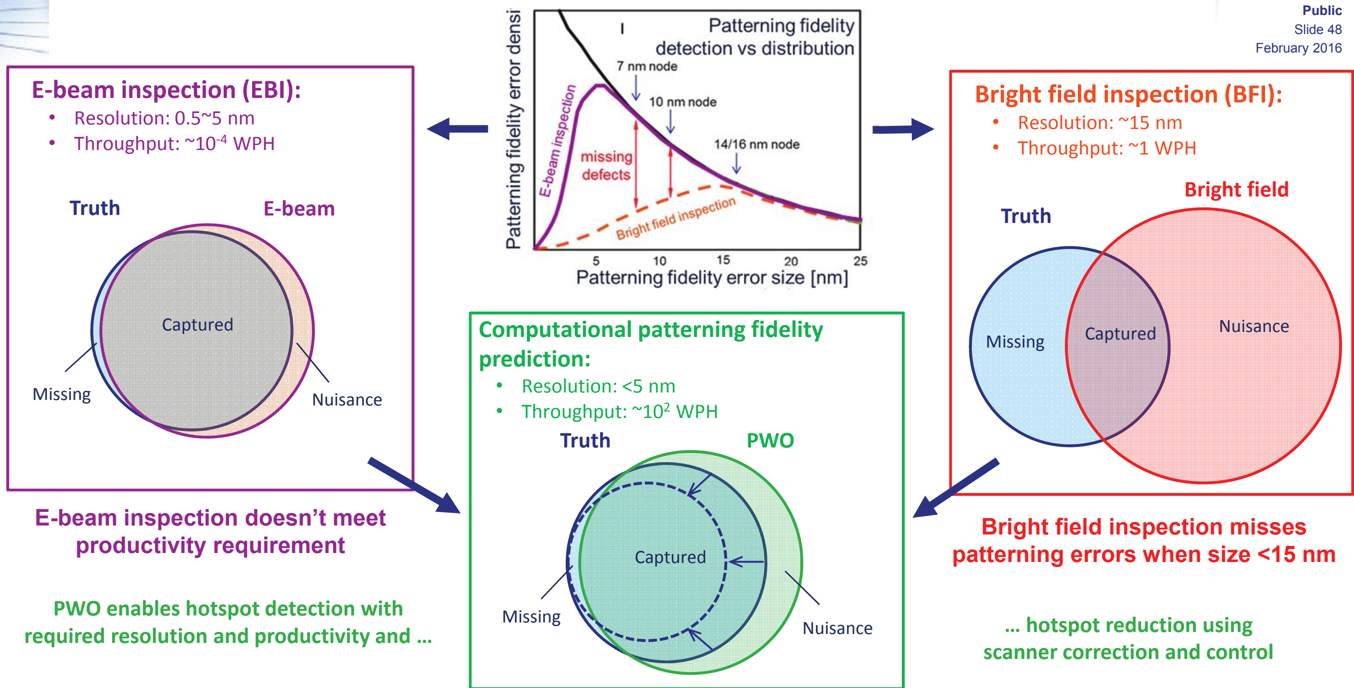
2 wafer data
No spacer control
Spacer control
Full wafer
3σ=0.7nm
Mean=-2.96nm
3σ=0.66nm
Mean=-2.46nm
3σ=0.41nm
Mean=-2.53nm
3σ=0.44nm
Mean=-2.35nm
S1-S2
0.70nm → 0.44nm
47% improved
Interfield FP
3σ=0.50nm
R²=0.70
3σ=0.41nm
R²=0.67
3σ=0.20nm
3σ=0.21nm
S1-S2
0.50nm → 0.21nm
58% improved
Intrafield FP
3σ=0.34nm
R²=0.98
3σ=0.35nm
R²=0.98
3σ=0.22nm
3σ=0.24nm
S1-S2
0.35nm → 0.24nm
31% improved
J. Lee et. al, "Spacer multi-patterning control strategy with optical CD metrology on device structures" SPIE conference 9778-80, February 2016


Challenge in pattern fidelity and control
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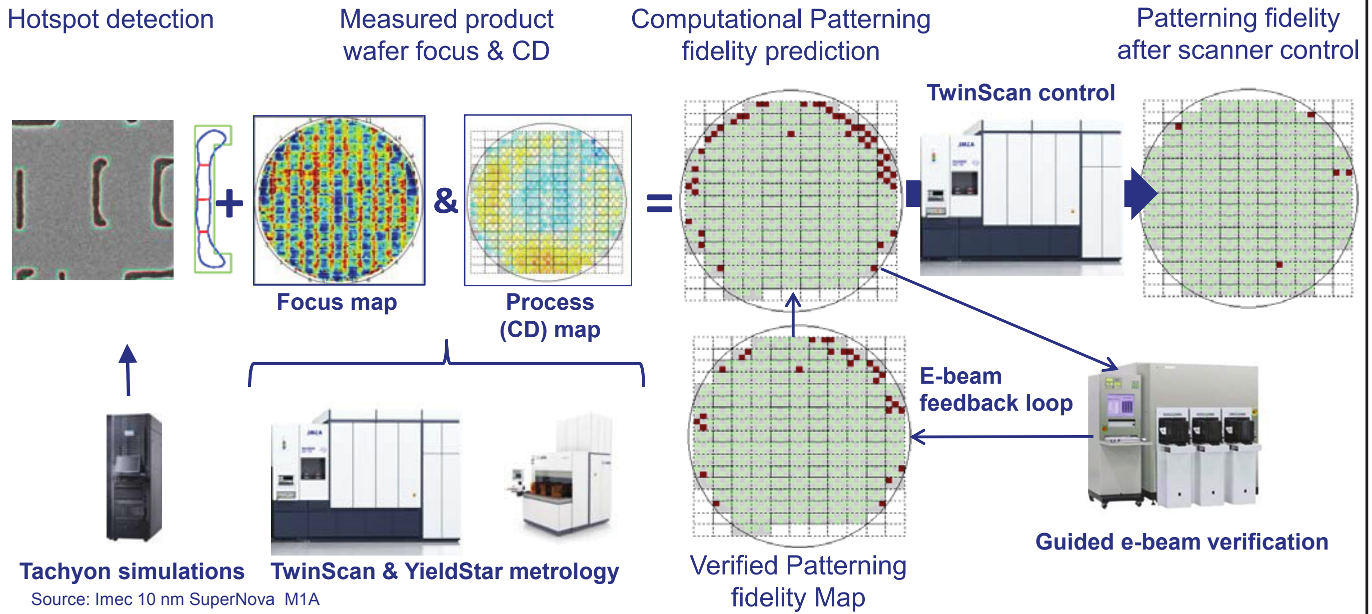
E-beam inspection (EBI):
Resolution: 0.5~5 nm
Throughput: ~10⁻⁴ WPH
Truth
E-beam
Captured
Missing
Nuisance
E-beam inspection doesn't meet productivity requirement
PWO enables hotspot detection with required resolution and productivity and ...
Patterning fidelity detection vs distribution
Patterning fidelity error densi
7 nm node
10 nm node
14/16 nm node
E-beam inspection
missing defects
Bright field inspection
Patterning fidelity error size [nm]
Computational patterning fidelity prediction:
Resolution: <5 nm
Throughput: ~10² WPH
Truth
PWO
Captured
Missing
Nuisance
Bright field inspection (BFI):
Resolution: ~15 nm
Throughput: ~1 WPH
Bright field
Truth
Missing
Captured
Nuisance
Bright field inspection misses patterning errors when size <15 nm
... hotspot reduction using scanner correction and control


Patterning fidelity litho control impact, the next holistic step
Using computational prediction allowing per wafer patterning control
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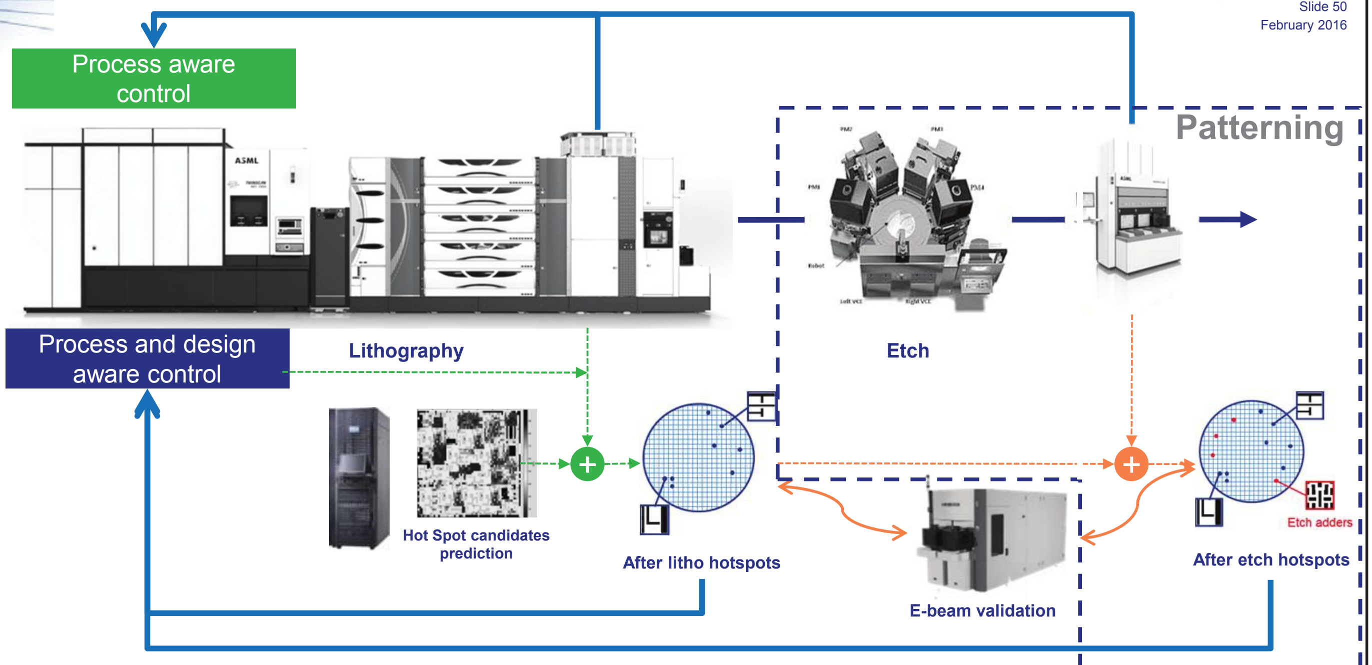
Hotspot detection
Measured product wafer focus & CD
Computational Patterning fidelity prediction
Patterning fidelity after scanner control
TwinScan control
Focus map
Process (CD) map
E-beam feedback loop
Guided e-beam verification
Tachyon simulations
TwinScan & YieldStar metrology
Source: Imec 10 nm SuperNova M1A
Verified Patterning fidelity Map


Extension of control loops to patterning and fidelity
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Process aware control
Patterning
Process and design aware control
Lithography
Etch
Hot Spot candidates prediction
After litho hotspots
E-beam validation
Etch adders
After etch hotspots

Pattern fidelity improvement through scanner corrections

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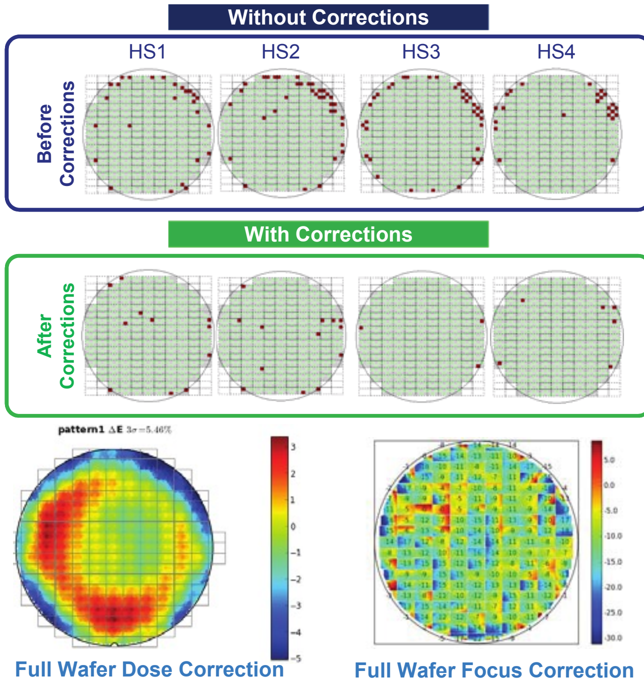

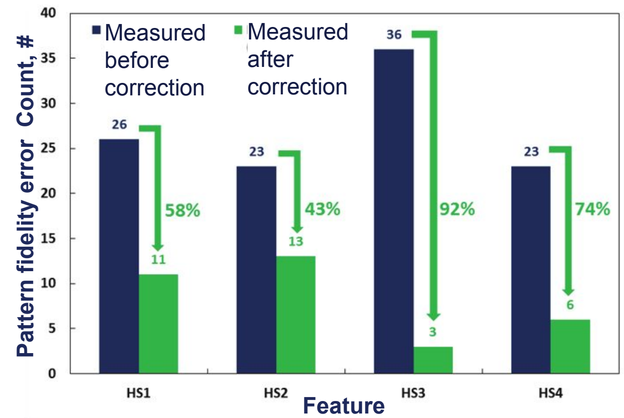

Marinus Jochemsen, Roy Anunciado, Vadim Timoshkov, Stefan Hunsche, Xinjian Zhou, Chris Jones, Neal Callan, "Process window limiting hot spot monitoring for high volume manufacturing" SPIE conference 9778, February 2016

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- 43 years overlay metrology in microlithography: How did we get here?
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Future trends in holistic lithography – overlay

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- In general for overlay and pattern fidelity:
  - The stepper correction capability is on a millimeter scale and underutilized
  - Sampling from product vs targets could lead to an different overlay measurement
- What we observe for overlay:
  - Overlay contribution from wafer deformation and marker fidelity vs stepper accuracy is increasing in the total overlay budget
  - Wafer deformation and marker fidelity variation from wafer to wafer starts contributing in the overlay
- As a consequence for overlay
  - There needs to be a consistent trend down in cost per measurement for metrology to allow higher sampling density
  - Sampling schemes need to be optimized capturing the relevant parameter instability and allow averaging to reduce noise
  - Above will allow scanner correction capability moving from feedback per batch on global targets to feedback per wafer on intra-die product structures

Future trends in holistic lithography – pattern fidelity

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- What we observe for pattern fidelity
  - Multiple patterning complexity increases the pattern variability per wafer not to be captured by existing tools for acceptable cost
  - The variability widens from variability in CD to variability in 3D geometry including edge placement and defects
- Pattern fidelity requirements could be met by
  - Optical CD metrology allows chip manufacturers to increase sample rate for acceptable cost allowing scanner correction capability per die per wafer
  - Defects could be predicted by simulating hotspots and convolutes with wafer focus, dose and aberration maps producing a per wafer defect probability map
  - Per wafer control loops can be designed for defect and edge placement by driving the stepper settings

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