# Epitaxially grown vertical junction phase shifters for improved modulation efficiency in silicon depletion-type modulators

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## ABSTRACT

High-speed silicon modulators based on the plasma effect in reverse-biased p(i)n junction phase shifters have been extensively investigated. The main challenge for such modulators is to maximize their modulation efficiency without compromising high-speed performance and insertion losses. Here, we propose a highly efficient silicon modulator based on a Mach-Zehnder Interferometer in which the doping profile of a vertical pin junction is precisely controlled by means of in-situ doping during silicon epitaxial growth. The precise level of control afforded by this fabrication procedure allows separately optimizing doping concentrations in the immediate vicinity of the junction and in surrounding electrical transport layers at the nanometric scale, enabling high performance levels. Free carrier absorption losses are minimized by implementing high carrier densities only in the waveguide regions where they benefit the most, i.e., in the immediate vicinity of the junction. Since these devices rely entirely on single crystal silicon, performance degradation caused by poor transport and high optical losses in poly- or amorphous silicon (as utilized in similar vertical phase shifter geometries such as semiconductor-insulator-semiconductor capacitive phase shifters) is avoided. Furthermore, unlike conventional plasma effect silicon phase shifters, the bandwidth of the proposed phase shifters is largely independent of the applied reverse voltage and the phase shift versus applied voltage is linearized, making them more suitable for complex modulation formats. The efficiency of the single ended phase shifters is expected to reach a $V_\pi L$ of 0.56 V·cm and absorption losses of $\alpha$=4.5 dB/mm, a good performance metric for depletion-type modulators. Lumped element Mach-Zehnder Modulators as well as travelling-wave modulators with phase matching based on meandered waveguides have been designed and their RF characteristics simulated and optimized with Ansoft HFSS. First experiments have validated the growth of the epitaxial stack and complete devices are currently being fabricated.

**Keywords:** Silicon Photonics, Integrated Optics, Electro-Optic Modulation, Optical Interconnects.

## 1. INTRODUCTION

Substantial growth of global data throughput in the last decade has motivated consequential efforts to further develop low power consumption, high-speed and low-cost optical transceivers for short distance and long haul data transmission links. Silicon Photonics (SiP) as a nascent technology compatible with complementary metal oxide semiconductor (CMOS) technology provides a low-cost platform [1-2], which allows for co-integration of passive and active photonic devices, as well as co-integration of photonics with electronics [3]. Since the electro-optic modulator plays a central role in any optical interconnect system, jointly achieving low drive voltage requirements, low power consumption and low insertion losses is an important goal for the research community, with high linearity playing a further role for longer reach communication systems with complex modulation schemes.

The plasma-effect in depletion-type reverse-biased p(i)n junctions has established itself as the mainstream actuation mechanism for high-speed SiP modulators [4]. The performance of such devices has advanced significantly in the past few years both in terms of bandwidth and optical loss. However, typical drive voltages to achieve complete extinction typically remain on the order of several volts preventing full extinction when driving with low cost high-speed CMOS electronics. Moreover, the voltage dependent capacitance of the phase shifters results in a nonlinear transfer function, limiting their compatibility with higher order modulation schemes. Efforts are still under way to improve both performance metrics. Very high doping of p(i)n phase shifters and thus reduced space charge regions

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alleviates both problems. The modulator behaves more linearly once the widths of the variable space charge regions significantly drop below that of the intrinsic region, with the stabilized junction capacitance then primarily determined by the latter. Moreover, the capacitance will be increased for small intrinsic and space charge regions, and thus the modulation efficiency will also be improved, since the effective refractive index change is the direct result of charge displacement inside the phase shifter. The drawback is quite obviously very high optical insertion losses due to high free carrier absorption. Although it is possible to shorten the device in order to keep the optical loss at an acceptable level, $V_\pi L$ scales unfavorably compared to free carrier induced losses with increasing doping concentrations, limiting the scaling of this approach.

In this work, we suggest a novel method for dopant distribution engineering inside the phase shifter, which allows for high doping levels close to the diode junction inside the phase shifter while maintaining the optical absorption losses relatively small. In the next section we introduce the design concept of the proposed phase shifter. Next, the fabrication of the phase shifter using epitaxial growth of in-situ doped silicon layers is discussed and metrology data from secondary ion mass spectrometry (SIMS) performed on a fabricated doped silicon stack reported. Finally, the designs of two modulators based on the proposed phase shifter, a short lumped element and a longer travelling wave modulator, are described and their simulated performance reported.

## 2. PHASE SHIFTER FABRICATION MODEL

In order to reduce the drive voltage and increase the modulation efficiency of depletion-type phase shifters two approaches are possible. The first is to increase the doping concentration of the p(i)n junction to reduce the space charge regions, increase the capacitance and thus enhance the number of transported carriers per applied voltage. The drawback consists in high optical losses due to free carrier absorption. They have limited doping levels in depletion-type phase shifters to less than ~2e18 $cm^{-3}$ [4]. The second approach is to increase the overlap between the optical mode and the variable space charge region. In a typical waveguide geometry in which the width exceeds the height, a vertical structure offers a higher overlap and higher modulation efficiencies [5]. However, formation of such phase shifters usually necessitates deposition of a poly- or amorphous silicon layer to contact the phase shifter, resulting in higher insertion losses [6,7]. Both high doping and vertical junctions in fully crystalline silicon can be achieved with the level of control over dopant concentrations afforded by in-situ doping, as explained in this section.

### 2.1 Phase shifter concept

While higher doping levels generally result in a higher modulation efficiency, they also translate into higher free carrier absorption. The product of the free carrier absorption losses $\alpha$ with the drive voltage, quantified by the associated figure of merit $\alpha \cdot V_\pi L$, scales unfavorably at higher doping levels. For example, increasing the n- and p-doping levels by a factor 5 in the phase shifter shown in Fig. 1(a), from n,p=5e17 $cm^{-3}$ to n,p=2.5e18 $cm^{-3}$ (both reasonable doping levels [8,9]) results in the effective index change $\Delta n_{eff}$ increasing from 8e-5 to 16e-5 for a 2 $V_{pp}$ reverse voltage swing and optical losses increasing from 1.2 dB/mm to 7.1 dB/mm (assuming the width of the intrinsic region to be 20 nm, the height of the waveguide to be 220 nm and the etch depth to be 120 nm). The loss increases by a factor 6 while $\Delta n_{eff}$ is only doubled. The two quantities scale differently since the variation of the depletion region width ($\Delta W_{Dep}$) versus applied reverse voltage decreases at higher doping levels, resulting in a reduced overlap with the region in which the free carrier concentration and thus the refractive index is modulated, while waveguide losses scale directly with the dopant concentration assuming most of the waveguide to be doped.

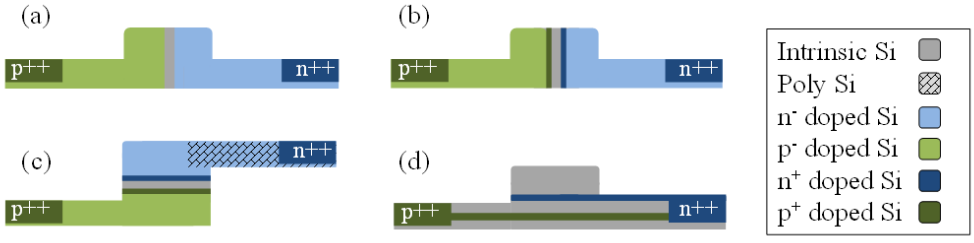


Fig. 1: schematic of different depletion-type phase shifter configurations. (a) Horizontal junction (b) horizontal junction with highly doped regions in the vicinity of the junction (c) vertical junction with narrow highly doped regions in the vicinity of the junction and top contacting with amorphous silicon, and (d) proposed phase shifter.

This suggests that the highly doped region should be present only in the vicinity of the depletion region and not in the whole phase shifter waveguide cross section. The structure in Fig. 1(b) illustrates this concept. As an example, if the doping concentrations are set to $n^+$,$p^+$=2.5e18 $cm^{-3}$ within 15 nm of the 20 nm wide intrinsic region and the rest of the waveguide is doped with $n^-$,$p^-$=5e17 $cm^{-3}$ simulations show an optical loss of 1.7 dB/mm (only slightly higher than for the low doped version of Fig. 1(a)) and a $\Delta n_{eff}$ of 16e-5 (same as for the highly doped version of Fig. 1(a)), resulting in a significant improvement. Since this structure is impractical to fabricate, alternative implementations have to be explored. Figure 1(c) shows a cross section of a modulator translating the same concept in a vertical junction. This structure can be fabricated e.g. by means of epitaxial growth of in-situ doped silicon, allowing sufficient control over the doping profile as experimentally shown in section 2.3. The thickness of each layer can be controlled in a range down to a few nanometers, since epitaxial growth of silicon is a relatively slow process. However, the structure shown in Fig. 1(c) requires a planarization process and deposition of poly- or amorphous silicon on top of the phase shifter and the surrounding oxide cladding in order to define the top contact. Polycrystalline and amorphous silicon are suboptimum in terms of optical losses per material conductivity [6,7]. The structure shown in Fig. 1(d) on the other hand does not require an additional poly- or amorphous silicon layer, since the thin $p^+$ and $n^+$ layers defining the pin diode can also be used for electrical contacting. Most of the volume of the phase shifter is left undoped. Therefore, higher implantation levels up to 1e19 $cm^{-3}$ can be implemented and high modulation efficiency is achievable without excessive free carrier absorption losses.

### 2.2 Fabrication process

The vertical junction depicted in Fig. 1(d) can be fabricated by means of epitaxial growth of in-situ doped silicon stacks. In-situ doping during chemical vapor deposition (CVD) of epitaxial silicon layers makes it possible to fabricate silicon stacks with thin highly doped layers with high dopant activation. It does not add ion-implantation mediated damage to the crystalline structure of the silicon, which can result in enhanced dopant diffusion, additional optical losses and lead to complications during epitaxial overgrowth. Compared to ion-implantation, in-situ doping gives much more control over the doped layer thicknesses, particularly for Boron for which the formation of highly doped shallow wells with ion-implantation technology is particularly difficult. Moreover, in-situ doped silicon does not require dopant activation and thus the thermal exposure after deposition of in-situ doped layers is limited to the subsequent silicon deposition (at 800°C). The anticipated process flow is shown in Fig. 2, starting with silicon-on-insulator (SOI) wafers with a 2 µm buried oxide and a 220 nm thick silicon device layer. After thinning down the device layer to 50 nm by thermal oxidation followed by wet etching in a buffered HF solution, the crystalline silicon is homogenously deposited by CVD using disilane as a precursor at a temperature of 800°C with a deposition rate of about 5 nm/min. Dopants are added by introducing diborane ($B_2H_6$) and phosphine ($PH_3$) gases to the chamber, respectively for p- and n-doping. The total thickness of the deposited silicon stack is chosen to be 290 nm. Waveguides are defined by etching the top silicon asymmetrically by respectively 200 nm and 150 nm on the p- and n-contact side. In order to increase the device bandwidth and minimize the power consumption, it is desirable to restrict the capacitor to the waveguide region. This is achieved by the deeper etch on the p-contact side. Unfortunately, in this process flow the capacitor is extended up to the $n^{++}$ well on the n-contact side, resulting in a suboptimum capacitance.

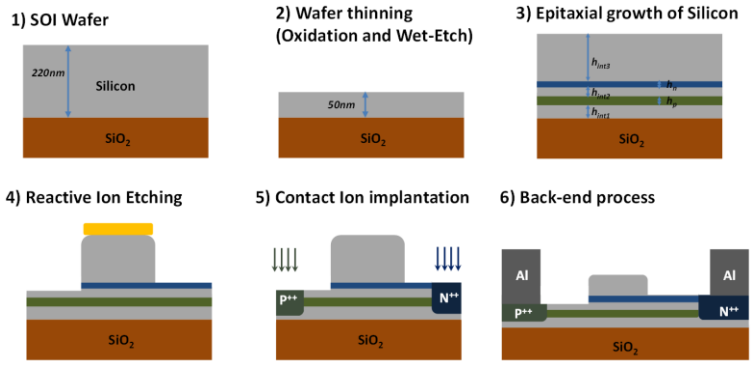


Fig 2. Illustration of the fabrication flow (wafer thinning, epitaxial growth, waveguide definition, implantation of contact wells followed by aluminum sputtering and a lift-off process for contact definition).

Once the waveguide is formed, $p^{++}$ and $n^{++}$ wells are formed on either side of the waveguide by ion implantation with concentrations of ~1e20 $cm^{-3}$ (sufficient to overcompensate overlapping $p^{+}$ doping in the case of the $n^{++}$ well) to provide an ohmic contact between the silicon and the metal. In order to obtain acceptable contact well mediated excess waveguide losses while maintaining an adequate RC bandwidth, the p- and n-wells are defined 600 nm and 800 nm from the waveguide edge, respectively. Subsequently, aluminum contacts are deposited by means of sputtering with a thickness of 2 μm and patterned with a lift-off process. Fig. 2(6) shows the final cross section of the modulator.

### 2.3 Experimental validation of the concept

To verify the accuracy and feature sizes that can be reached for the doping distribution, we experimentally validated the epitaxial growth process, with characterization results of a process calibration run shown in Fig. 3. Rutherford Backscattering Spectrometry (RBS) measurements were performed in both random and channeling mode utilizing 1.4 MeV $He^{+}$ ions at a scattering angle of 170°. Due to the low atomic concentration of the dopants, only silicon atoms contribute to the random spectrum in Fig. 3(a). The channeling spectrum of the epitaxially grown silicon stack displays no difference to that of a bulk silicon wafer, showing the grown layers to have a high crystalline quality. The minimum channeling yield $\chi_{min}$, defined as the ratio between channeling and random spectra for energies below the surface peak, amounts to about 4 %, indicating an excellent substitutionality of the silicon atoms. To determine the electrically active carrier concentrations in the grown layer, electrochemical capacitance-voltage (ECV) measurements were performed, as shown in Fig. 3(b). The measured thicknesses and doping profiles match the targeted geometry (inset of Fig. 3(a)) and demonstrate the high level of control over layer thicknesses and dopant concentrations.

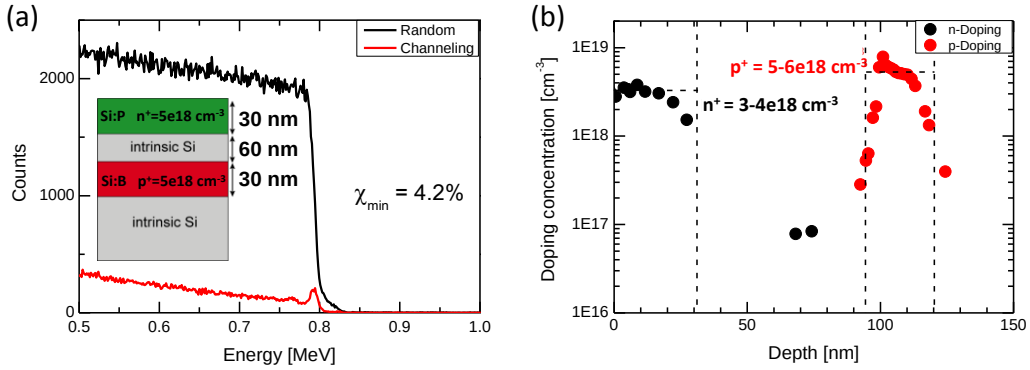


Fig. 3. (a) Rutherford backscattering spectrometry (RBS) measurements performed on the grown epitaxial stack. The inset shows the targeted geometry. (b) Doping profile of the silicon stack from Electrochemical Capacitance-Voltage (ECV) measurements.

## 3. DEVICE DESIGN

### 3.1 Phase shifter design

The targeted doping levels of the p- and n-doped regions inside the rib waveguide are the result of a tradeoff between total optical loss, modulation efficiency and electro-optic cutoff frequency. Figures 4(a) and 4(c) show the calculated $\Delta n_{eff}$ and optical loss for a 2 $V_{pp}$ voltage swing applied to the phase shifter (0 V to 2 V reverse bias) versus donor and acceptor concentrations $N_d$ and $N_a$. The thickness of the intrinsic layer is $h_{int}$=50 nm, the thicknesses of p- and n-doped layers are respectively 30 nm and 20 nm. The modulator length required to achieve π/2 phase shift (assuming a dual drive Mach-Zehnder Modulator (MZM) operated in push pull configuration) is then evaluated as $L_{\pi/2} = \lambda/(4\Delta n_{eff})$ (Fig. 4(b)) and the resulting insertion losses calculated (Fig. 4(d)). The calculated 3 dBe intrinsic cutoff frequency of the phase shifter ($f_c=1/2\pi RC$) also improves at higher doping levels (Fig. 4(e)), since the capacitance asymptotically converges to that of a parallel plate capacitor with a spacing $h_{int}$ between the electrodes, while the series resistance continues to drop at high doping levels.

A dual drive lumped element MZM with a drive voltage chosen to achieve full extinction and a length sized to reach 1 dB of waveguide losses has a power consumption given by $C_L \cdot V_\pi L^2 \cdot \alpha/8$ [10], where $C_L$ is the capacitance per unit length and α is in units of dB/length. We introduce the figure of merit FOM = $\Delta n_{eff}^2 \cdot f_c/(\alpha C_L)$ proportional to the

product of the inverse of the aforementioned power consumption with the intrinsic phase shifter bandwidth $f_c$. For the layer thicknesses described above, $N_d$=4e18 cm$^{-3}$ and $N_a$=8e18 cm$^{-3}$ maximize the figure of merit (Fig 4(f)).

This high doping levels result in a phase shifter with a relatively high capacitance of 1.62 nF/m and a low series resistance of 2.29 mΩ·m (both at 0 V), which results in a 42 GHz intrinsic bandwidth. The free carrier absorption losses are 4.5 dB/mm (also at 0 V). Applying a 2 V reverse bias to the phase shifter results in an effective index change of 2.7e-4, which requires a length of 1.4 mm to achieve a π/2-phase shift ($V_\pi L$=0.56 V·cm).

The cross section of the optimized silicon stack is shown in Fig. 5(a). We have also fabricated this layer stack with the process described in section 2.2. RBS measurements (Fig. 5(b)) confirm very high quality deposited silicon layers. The actual spatial carrier distribution was determined by an ECV measurement (Fig. 5(c)), which is in good agreement with the targeted structure. The tail of the n-dopants reaching inside the nominally intrinsic top silicon capping layer can be due to residual dopants inside the chamber and phosphorus segregation at the surface, since we did not interrupt the growth process for gettering the Phosphorous out of the chamber.

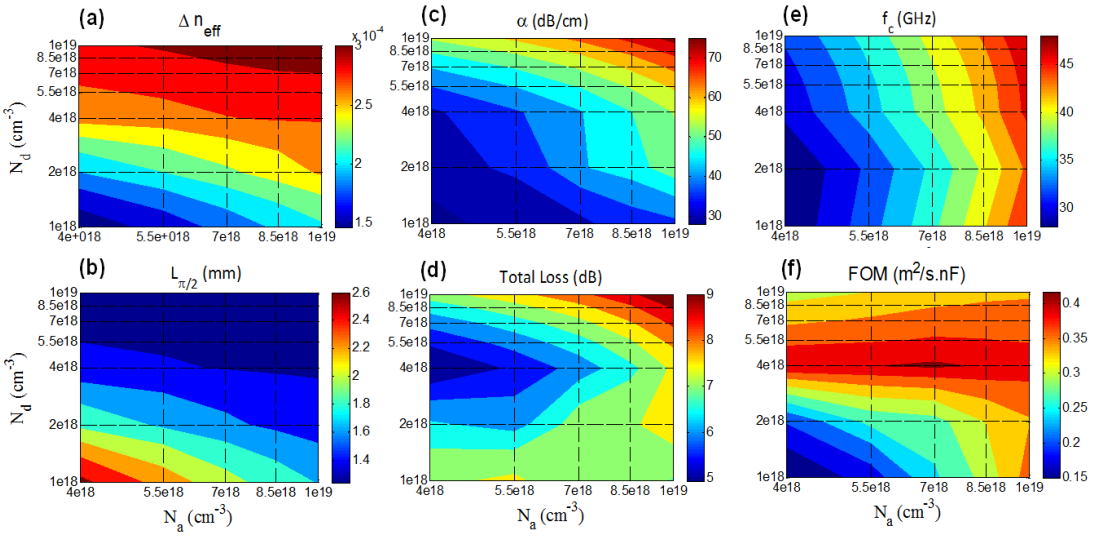


Fig. 4. (a) Effective index change between 0 V and 2 V reverse bias, (b) $L_{\pi/2}$ derived from (a), (c) optical loss per unit length, (d) total loss for a phase shifter reaching π/2 phase shift, (e) intrinsic cutoff frequency 1/2πRC, and (e) the FOM $\Delta n_{eff}^2 \cdot f_c/(\alpha C_L)$.

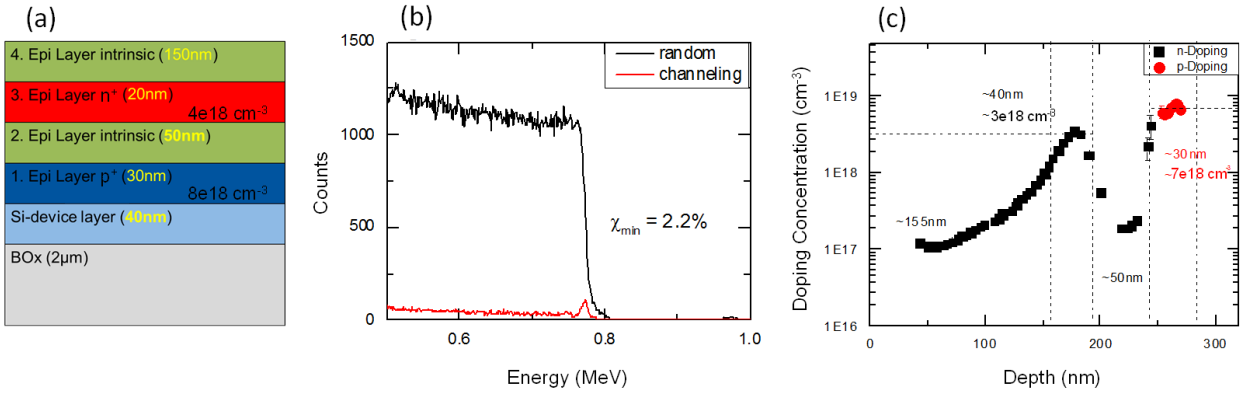


Fig. 5. (a) Cross section of the targeted silicon stack, (b) RBS measurements and (c) doping profile of the stack as determined by ECV measurements.

In the next section, the layout and the simulated performance of a lumped element and a travelling wave modulator relying on the proposed phase shifter are reported.

### 3.2 Lumped element modulator

For a lumped element modulator (i.e., a short modulator relative to the RF wavelength in the structure, here with a length on the order of 1/10$^{th}$ of the RF wavelength) the cutoff frequency of the device will be only limited by the RC time constant. Therefore, similar scaling of the linear capacitance $C_L$ and the inverse linear diode series resistance $1/R_L$ will not affect the *intrinsic* bandwidth. On the other hand, a higher capacitance results in higher modulation efficiency. Moreover, the short device length makes it less sensitive to waveguide losses. Thus, lumped element modulator designs naturally gravitate towards high doping levels, a high capacitance and a low resistance. In that design space, the output impedance of the driver $Z_{dri}$ plays a crucial role since the series resistance of the modulator is small and $Z_{dri}$ plays a substantial role in the total series resistance. For instance, for the MZM shown in Fig. 6(a) which is 250 µm long, the total series resistance of one modulator arm is 9.2 Ω. Thus, a driver output impedance of $Z_{dri}$=10 Ω (Fig 6(b), blue curve), halves the intrinsic analog bandwidth. Reducing the driver impedance to a low but still realistic value $Z_{dri}$=4 Ω results in a bandwidth of 35 GHz at 2 V bias. The performance metrics of the device are summarized in table 1.

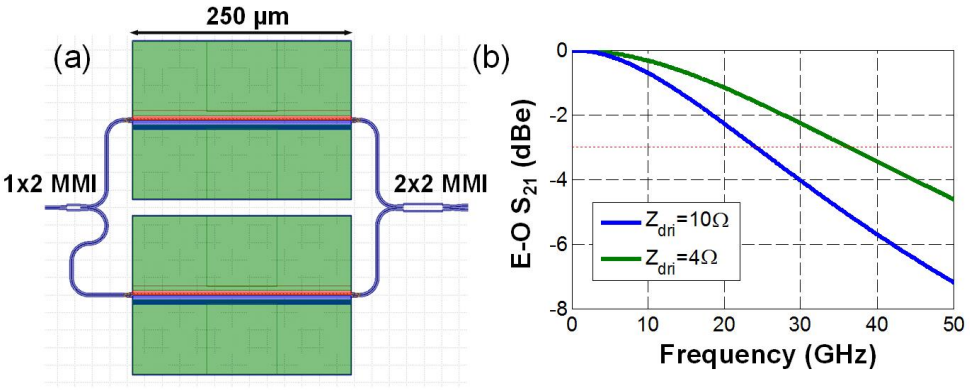


Fig. 6. (a) Layout of the 250 µm lumped element MZM. The red and blue layers respectively represent p- and n-doped wells, the green layer represents metal electrodes. (b) Electro-optic $S_{21}$ of the lumped element MZM for two driver output impedances.

### 3.3 Travelling wave modulator

In order to further reduce the required drive voltage, longer phase shifters are required. Figure 7 shows the layout of a travelling wave modulator in which the length of the waveguide is 1.4 mm. To achieve a high cutoff frequency, phase matching between the group velocity of the optical mode and the RF signal must be verified. To slow down the optical wave and obtain phase matching, we have increased the optical path length by meandering the waveguide. Metal extensions contact the metal lines to the waveguide, reducing the series resistance of the loaded transmission line (and thus reducing transmission line losses and increasing the electro-optic bandwidth) without increasing the fringe capacitance between the metal lines or significantly changing the RF index [11-12]. As in Fig. 6, the red and blue layers respectively represent the p- and n-doped wells. The high-speed performance of the device

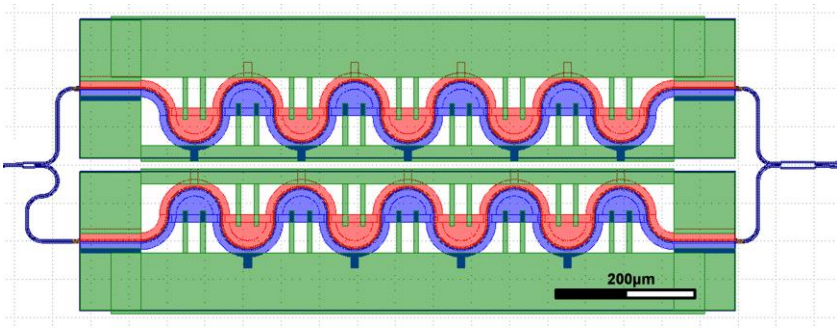


Fig. 7. Layout of the travelling wave modulator.

is calculated and the phase matching verified by means of the commercial finite element method solver HFSS from Ansys. The simulation results predict a cutoff frequency of 21 GHz mainly limited by RF losses in the transmission line. Since achieving a characteristic impedance of 50 Ω is very challenging due to the high capacitive load applied to the transmission line [12], the travelling wave modulator is designed for a 25 Ω system, which is also beneficial in terms of RF losses at the cost of increased power consumption [11-12].

Table 1. Performance metrics of the travelling-wave and the lumped element modulators using the proposed phase shifter.

| Device Type | Phase Shifter Length | -3 dBe Bandwidth | Insertion Loss | Drive Voltage for full extinction | Optimum Driver Output Impedance |
|---|---|---|---|---|---|
| Travelling-wave MZM | 1.4 mm | 21 GHz | 6.3 dB | 2.0 Vpp | 25 Ω |
| Lumped Element MZM | 250 µm | 35 GHz | 1.2 dB | 11 Vpp | $\leq$ 4 Ω |

## 4. CONCLUSION

We propose a depletion-type vertical phase shifter fabricated by means of in-situ doped epitaxially grown crystalline silicon. This method yields high control over the dopant distribution inside the phase shifter. A high modulation efficiency of 0.56 V·cm is achieved from a combination of high mode overlap in the vertical structure and high doping levels. Most of the phase shifter volume is left undoped, resulting in moderate free carrier absorption losses of 4.5 dB/mm given the high doping levels. The characteristics of a lumped element modulator as well as a longer travelling wave modulator based on the proposed phase shifter are summarized in table 1.

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