Direct surface nanopatterning using pyramidal silicon nanopore arrays as templates

Tao Deng
Jian Chen
Mengwei Li
Chenxu Zhao
Zewen Liu

Direct surface nanopatterning using pyramidal silicon nanopore arrays as templates

Tao Deng
Jian Chen
Mengwei Li
Chenxu Zhao
Zewen Liu
Tsinghua University
Institute of Microelectronics
Beijing 100084, China
E-mail: liuzw@tsinghua.edu.cn

Abstract. Template-based surface nanopatterning techniques are highly efficient methods in realizing different surface nanopatterns, which are the fundamental structures of various nanodevices. We demonstrate a template of pyramidal silicon nanopore array (PSNA) for direct surface nanopatterning. Using the PSNA templates, deposition experiments of platinum (Pt) and gold-palladium (Au-Pd) particles on chromium-coated silicon substrates were performed. Individual Pt nanocubes and nanocube arrays with different shapes and feature sizes as small as 82 nm were obtained. By tuning the gap between the PSNA template and the substrate, Au-Pd microdot arrays with an average diameter of 7.6 μm were also fabricated. As the nanopore size and shape of the PSNA template can be easily controlled, the corresponding size and shape of the transferred surface nanopatterns are tunable. These results indicate the potential of the PSNA templates for large-scale production of nanopatterns with desired sizes and shapes. © *The Authors. Published by SPIE under a Creative Commons Attribution 3.0 Unported License. Distribution or reproduction of this work in whole or in part requires full attribution of the original publication, including its DOI.* [DOI: 10.1117/1.JMM.12.4.041307]

Subject terms: surface nanopatterning; nanopore array templates; deposition; nanocubes.

Paper 13094SS received Jun. 21, 2013; revised manuscript received Aug. 29, 2013; accepted for publication Sep. 9, 2013; published online Oct. 18, 2013.

1 Introduction

Over the past decades, the smallest feature size of integrated circuits has become smaller and smaller. Nowadays, it has decreased to 22 nm. During this process, surface nanopatterning has become one of the most intensively studied topics in the fields of material science and engineering. There are different nanostructuring techniques in patterning various building blocks (e.g., nanodots, nanopillars, nanorods, nanospheres) on the surface of substrates, mainly including lithographic methods,[1] nanoimprinting[2] and replica molding processes,[3] scanning probe microscope (SPM) writing techniques,[4] and template-based methods.[5,6] Among these techniques, surface patterning methods using templates are highly efficient in preparing surface nanostructures. Compared to the lithographic methods including normal lithography, electron-beam lithography, even ArF immersion lithography and EUV lithography, the template-based methods are time-saving approaches with low equipment cost in fabricating large-scale ordered arrays of surface structures because they do not require any resists.

Among the various templates that have been used to prepare surface patterns on substrates, there are three widely used templates: ultrathin alumina membranes (UTAMs),[7,8] monolayer polystyrene (PS) sphere arrays,[9] and block copolymer (BCP) patterns.[10] These templates have different morphological features: the UTAM porous template has parallel-aligned cylindrical nanopores, the PS template is a monolayer of closely packed arrays of spheres, and the BCP template has some special shapes such as lamella. The feature size of the building blocks of the surface patterns prepared using UTAM, PS, and BCP templates can be adjusted within the range of about 5 to 500 nm, 50 to 4.5 mm, and 5 to 50 nm, respectively. Considering the smallest feature size,

the variable size range, the large pattern area (>1 cm^2) and ultrahigh density (10^{10} to 10^{12} cm^{-2}), the UTAM template is the most promising option to meet the industrial requirements of size minimization of surface patterns (device miniaturization). Using UTAMs as deposition,[11–13] etching,[14–17] and replication masks,[18–20] diverse surface building blocks at nanoscale have been prepared.

However, there are two challenging points preventing the UTAM patterning in synthesizing regularly arrayed quantum-sized structures (<10 to 20 nm). First, when the pore diameter is less than 20 nm, the pore arrangement will become irregular. Second, UTAMs used for surface patterning should have pores with aspect ratio less than 10. For example, the thickness of an UTAM with 20-nm-diameter pores should be less than 200 nm. However, UTAMs that are thinner than 200 nm are difficult to be prepared due to the large growth rate of UTAMs.[6] In addition, the shapes of the building blocks prepared using UTAM templates are limited. It is almost impossible to fabricate rectangular nanostructures or nanowires using UTAM templates. In order to overcome the limitations of the UTAM templates, Altug and her coworkers proposed a novel template (nanostencil).[21] Using the nanostencils as deposition masks, they fabricated engineered infrared plasmonic nanorod antenna arrays with a feature size of 230 nm, which demonstrated comparable performance to that of arrays fabricated by electron beam lithography (EBL). Nevertheless, the nanostencils themselves were fabricated using EBL, which was both slow and expensive as each structure of the nanostencils was lithographically defined in a serial manner.

In this article, a novel surface nanopatterning template is demonstrated. The template is a pyramidal silicon nanopore array (PSNA), which can be fabricated using a combination

of dry and wet etching, or just a three-step wet etching, as shown in our previous work.[21–23] Therefore, the PSNA template fabrication steps and costs are significantly reduced. As the size and shape of the nanopore in the PSNA template can be easily tuned, the corresponding size and shape of the surface structures transferred from the template are tunable. Based on such PSNA templates, direct surface nanopatternings of platinum (Pt) and gold-palladium (Au-Pd) on chromium-coated silicon substrates by deposition were conducted. Individual Pt nanocubes and nanocube arrays with different shapes and feature sizes as small as 82 nm, as well as Au-Pd microdot arrays with an average diameter of 7.6 μm, were obtained.

2 Experimental Details

Figure 1 shows a schematic view of the deposition nanopatterning system, which consists of sputtered particles, a PSNA template, and a substrate. The mechanism of using a template to create surface patterns is to transfer the structural features of the template to the surface structures on substrates, obtaining surface patterns with similar morphological features to those of the template. In this deposition system, the PSNA template was placed on the sample substrate and had pores of various sizes and shapes through which sputtered particles were deposited on the substrate. Therefore, the nanopores in the template control the shape of the deposited patterns.

Another factor that may influence the morphology of the deposited patterns is the gap (H) between the template and the substrate. The template is normally placed directly on the substrate for patterning and deposition of nanoparticles. This step is also one of the ordinary resistless shadow masking methods used in metal patterning. In the case of metal patterning by thermal evaporation, the gap between the template and the substrate causes a defocusing effect to produce a blurred pattern larger than the template pore due to the geometrical projection of the beam of vaporized metal. In order to investigate the effect of the gap between the PSNA template and the substrate, two different types of gap built up by spacers were introduced: one had no spacer (0 μm) with the tip of the pyramidal nanopore directly contacting with the substrate (hereafter contact mode); the other one had a

500-μm-silicon sheet and the pyramidal nanopore was flipped over (hereafter spacer mode).

The PSNA templates were fabricated in a P-type (100) double-side-polished single crystalline silicon wafer using a combination of inductive couple plasma etching and a two-step anisotropic wet etching, as shown in our previous work.[22,23] In fact, such templates can also be prepared with an improved three-step wet etching process to further reduce the fabrication cost, as shown in our latest work.[24] Compared with other surface nanopatterning templates such as UTAM, the PSNA template has some unique advantages. First, the nanopore shape of the PSNA template can be easily controlled by changing the length-width ratio of the wet etching window. Second, the space between two nanopores of the PSNA template can be designed freely. Thus, various surface patterns with different shapes and different spaces can be created with the PSNA templates. Furthermore, PSNA templates are always robust enough to be reused because the thickness of the PSNA templates is always several micrometers.

The sputtered particles in the deposition experiments were platinum (Pt) particles and gold-palladium (Au-Pd) particles generated by a precision etching coating system (PECS 682, Gatan, Inc., CA). The deposition rate (coating rate) was 8.5 nm/min when the PECS was operating at 7 keV and 3×10^{-6} Torr. The substrates were silicon (Si) wafers coated with a layer of chromium (Cr), whose thickness was 300 nm. After the deposition experiments, the fabricated surface patterns were investigated using an environmental scanning electron microscope (ESEM, Quanta 200 FEG, FEI Company, OR) and a SPM (Nanoman VS, Veeco Company, NY). The spatial resolution of the ESEM and the SPM in typical modes was 2.1 and 0.3 nm, respectively.

3 Results and Discussions

3.1 PSNA Templates

As the nanopore morphology of the PSNA templates determines the sizes and shapes of the deposited surface nanopatterns, the PSNA templates were carefully fabricated and investigated. Figure 2 shows a 22×20 PSNA template and its details, where every black dot represents a nanopore. The pitch between two nanopores is 10.8 μm, which is much bigger than the typical space (tens to hundreds of nanometers) between two elements in UTAM templates. However, this problem can be easily solved by reducing the initial space between the wet etching windows during the template fabricating processes. Additionally, by placing the PSNA template on a manipulator, which allows precise three-dimensional (3-D) orientation of the template independent of the substrate, step-and-repeat nanopatterning with a space of several nanometers can be realized, just as Taylor et al. have done.[25]

From Fig. 2(b), it can be seen that the size of the nanopore in the ninth row and the eleventh column of the PSNA template is 151×189 nm^2. Further investigation indicates that the relative size error of the nanopores within the 22×20 array is less than 20%. However, the size uniformity in the PSNA template gets worse when the investigation area gets larger, especially when the area is over 1 cm^2, as shown in our previous work.[24] The problem of nanopore nonuniformity is mainly due to the thickness error of the
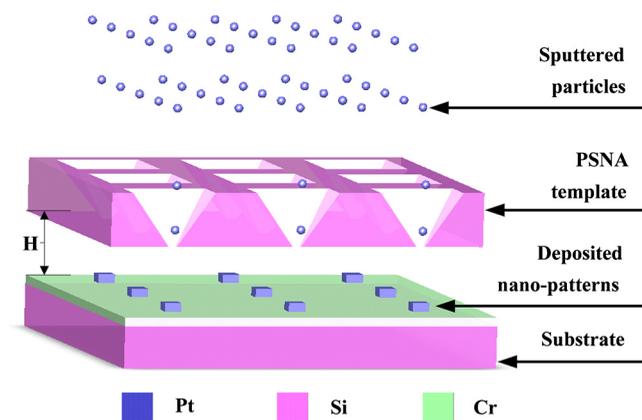

Fig. 1 Schematic illustration of the surface nano-patterning by deposition of platinum particles using the pyramidal silicon nanopore array (PSNA) as the template.
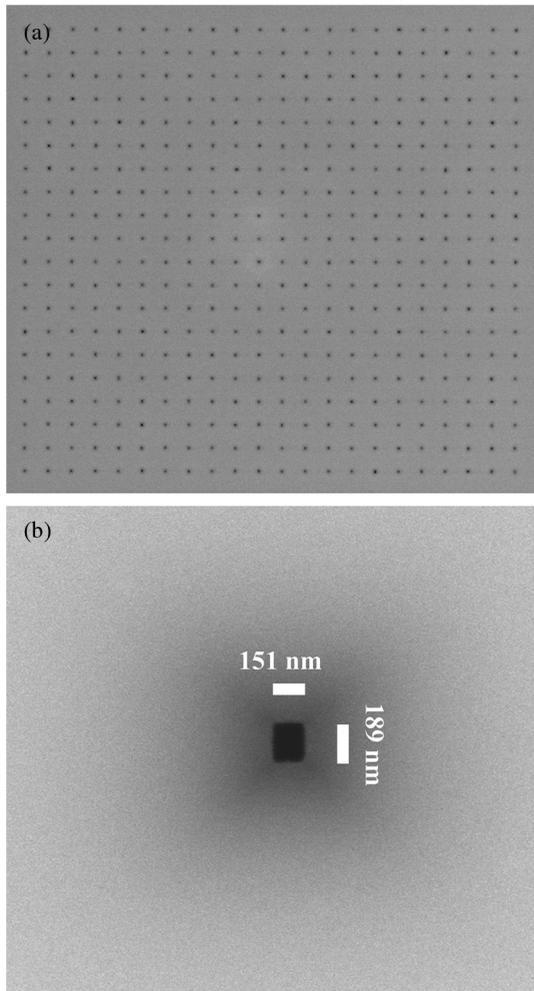
Fig. 2 SEM micrographs of a PSNA template and its details: (a) A 22 × 20 nanopore array in the PSNA template and (b) details of the nanopore in the ninth row and the eleventh column of the array.

common wafer (±10 μm within the 4 in. chip), the size error of the wet etching window, as well as the wet etching process errors. The nonuniformity of the PSNA template will surely transfer to the patterning structures. Therefore, the fabrication processes of the PSNA template should be carefully optimized. Silicon-on-insulator wafers will be used to improve the size uniformity of the PSNA templates in the near future.

3.2 *Nanostructure of Patterns*

Based on the assumption of pattern determination mainly by the gap between the template and the substrate when the size and shape of the template have been given, smaller patterns should be obtained with a smaller gap. Thus, the smallest patterns should be created when the deposition system is operating in the contact mode.

Figure 3 shows a 2 × 2 nanocube array created by the deposition of Pt particles on the Cr/Si substrate using a PSNA template operating in the contact mode. From Fig. 3(a), it can be seen that four nanocubes have been successfully fabricated on the substrate, where the pitch between two elements is 10.8 μm. Figure 3(b) shows that the size of the nanocube located in the lower left corner of the array is 169 × 203 nm^2,
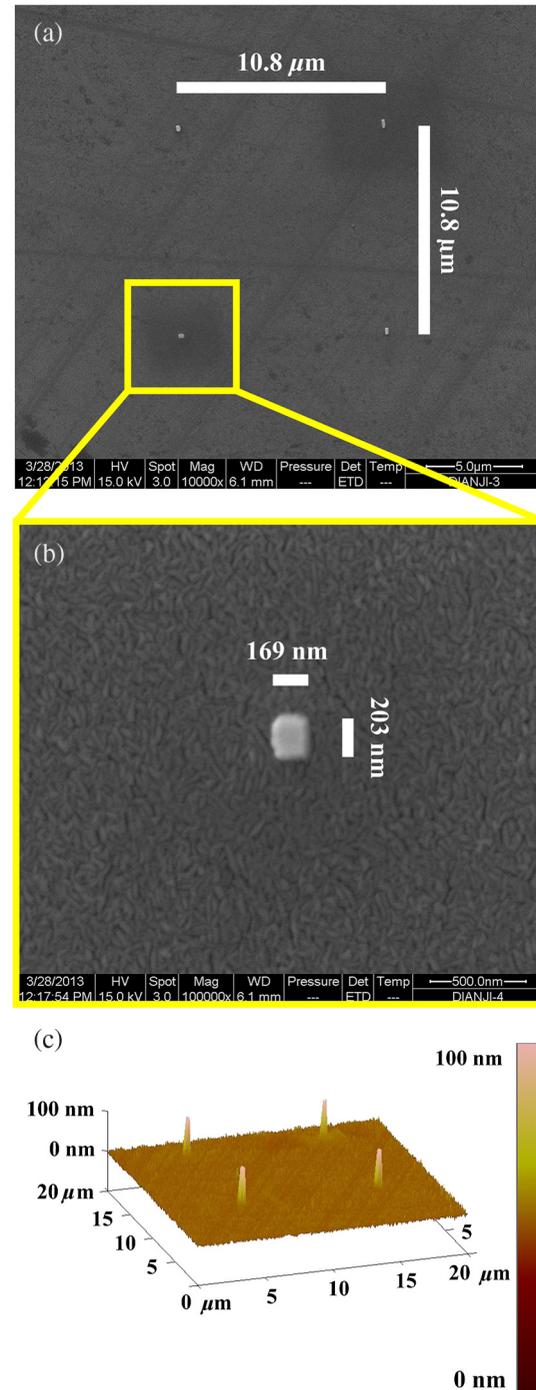

Fig. 3 Surface nanocubes created by the deposition of Pt particles on the Cr/Si substrate using a PSNA template operating in the contact mode: (a) and (b) SEM images of a 2 × 2 nanocube array and its details; (c) a AFM image of the array.

which is a little bigger than the size of the corresponding nanopore in the PSNA template [Fig. 2(b)]. Considering that some parts of the PSNA template and the substrate might not contact tightly, the little size difference is reasonable. Figure 3(c) demonstrates the 3-D topography of the 2 × 2 nanocube array; the average height of the nanocubes is 108 nm with a relative error of 9% while the roughness of the substrate (Cr/Si) is 7.27 nm. In fact, the adhesion layer (Cr) is not necessary since PSNA nanopatterning
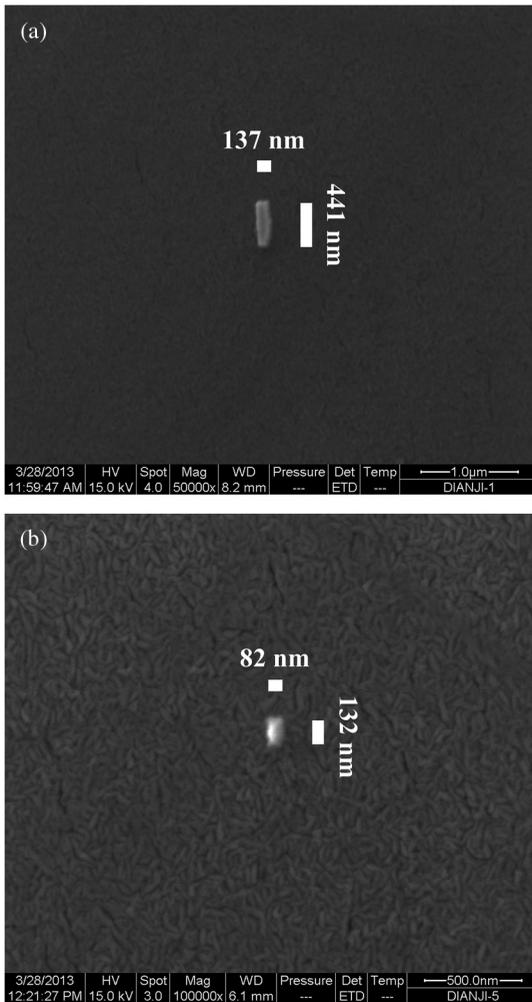
Fig. 4 Surface nanocubes created by deposition of Pt particles on the Cr/Si substrate using PSNA templates operating in the contact mode: (a) a nanocube with the size of 137×441 nm^2 and (b) a smaller nanocube with the size of 82×132 nm^2.

Fig. 5 Surface microdots created by deposition of Au-Pd particles on the Cr/Si substrate using a PSNA template operating in the space mode: (a) a 3×3 microdot array and (b) details of the microdot in the lower middle part of the array.

does not require metal lift-off processes. Without the Cr layer, the height error of the nanocubes would be reduced.

It is worth noting that the relative error of plane size of the nanocubes is 14% within the 2×2 array, whereas it is about 20% within the 22×20 array. This result indicates that the size uniformity of the nanopatterns gets worse when the observation area gets bigger. This phenomenon is consistent with the investigation of the size uniformity of the PSNA template (shown in our previous work[24]), which means that the poor size uniformity of the PSNA template is the main contribution to the nanopatterns' nonuniformity. Therefore, the size uniformity of the PSNA templates needs to be further improved to obtain uniform nanopatterns.

By utilizing other PSNA templates with smaller feature sizes and different shapes, different surface nanocubes were obtained, as shown in Fig. 4. Figure 4(a) shows a rectangular nanocube with the size of 137×441 nm^2, whereas a smaller nanocube with the size of 82×132 nm^2 is shown in Fig. 4(b). These results indicate that individual nanocubes and nanocube arrays with feature sizes of 80 nm can be successfully fabricated. Meanwhile, the shape of the deposited nanocube can be easily controlled by carefully designing the PSNA template. As pyramidal nanopores with different
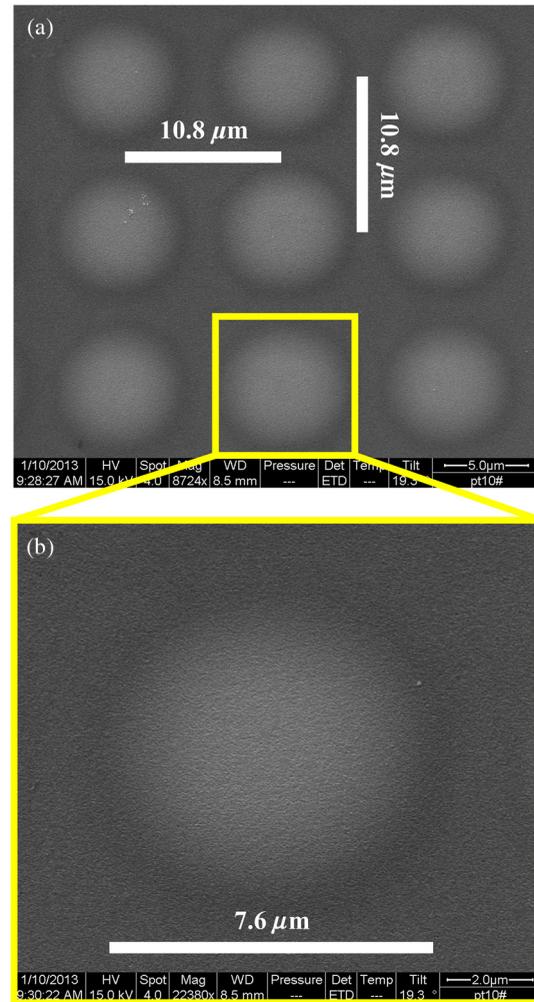
shapes (square, rectangle with different length-width ratio, even slit) and different sizes have been fabricated in our group,[21,25] it is promising that massive production of surface nanocubes and nanocube arrays with desired feature sizes and shapes, as well as synthesized nanodevices, can be achieved with the method proposed in this article.

3.3 Microstructure of Patterns

Figure 5 shows a 3×3 microdot array created by deposition of Au-Pd particles on the Cr/Si substrate using the upside-down PSNA template operating in the space mode. It can be seen that nine microdots have been successfully fabricated on the substrate, where the pitch between two elements is 10.8 μm. However, unlike the rectangular shape of the nanopores in the PSNA template [Fig. 2(b)], the shape of the deposited microdots is a circle. The detailed image of the microdot in the lower middle part of the array indicates that the deposited patterns in the space mode, which had a much larger gap (500 μm) compared to the thickness of the PSNA template (4.2 μm), were up to 7.6 μm and blurred, as shown in Fig. 5(b). This phenomenon is similar to the metal patterning by thermal evaporation using templates

and is the result of the geometrical projection of the metal particles' beam. The relative size error of the microdots within the 3×3 array is 8%, which is less than the relative size error of the nanocubes fabricated in the contact mode (14%). These results indicate that the deposition with the PSNA template can form identical microdots by one batch process, which has potential applications in plasmonic and photonic fields such as plasmon-based sources and microlens arrays.

4 Conclusions

A novel template of PSNAs for direct surface nanopatterning was demonstrated. Using this template, deposition experiments of platinum (Pt) and gold-palladium (Au-Pd) particles on chromium-coated silicon substrates were conducted. Individual Pt nanocubes and nanocube arrays with different shapes and feature sizes as small as 82 nm were obtained. By changing the gap between the template and the substrate, microdot arrays with an average diameter of 7.6 μm were also created. As the nanopore size and shape of the PSNA template can be easily controlled, the corresponding sizes and shapes of the transferred surface nanopatterns are tunable. These results indicate the potential of PSNA templates for the large-scale production of surface nanopatterns with desired sizes and shapes, at low cost and reduced steps.

References

1. J. A. Liddle and G. M. Gallatin, "Lithography, metrology and nanomanufacturing," *Nanoscale* **3**(7), 2679–2688 (2011).
2. Y. Yang et al., "Nanoimprinted polymer solar cell," *ACS Nano* **6**(4), 2877–2892 (2012).
3. G. L. W. Cross, "The production of nanostructures by mechanical forming," *J. Phys. D: Appl. Phys.* **39**(20), R363–R386 (2006).
4. K. Zhang et al., "Direct writing of electronic devices on graphene oxide by catalytic scanning probe lithography," *Nat. Commun.* **3**, 1194 (2012).
5. Y. Li et al., "Physical processes-aided periodic micro/nanostructured arrays by colloidal template technique: fabrication and applications," *Chem. Soc. Rev.* **42**(8), 3614–3627 (2013).
6. Y. Lei et al., "Surface patterning using templates: concept, properties and device applications," *Chem. Soc. Rev.* **40**(3), 1247–1258 (2011).
7. H. Masuda and M. Satoh, "Fabrication of gold nanodot array using anodic porous alumina as an evaporation mask," *J. Appl. Phys.* **35**(1B Part 2), L126–L129 (1996).
8. Y. Lei, W. Cai, and G. Wilde, "Highly ordered nanostructures with tunable size, shape and properties: a new way to surface nano-patterning using ultra-thin alumina masks," *Prog. Mater. Sci.* **52**(4), 465–539 (2007).
9. Y. Li, W. Cai, and G. Duan, "Ordered micro/nanostructured arrays based on the monolayer colloidal crystals," *Chem. Mater.* **20**(3), 615–624 (2008).
10. J. Bang et al., "Block copolymer nanolithography: translation of molecular level control to nanoscale patterns," *Adv. Mater.* **21**(47), 4769–4792 (2009).
11. M. Wu et al., "UTAM surface nano-patterning in fabricating quantum-sized nanodots," *Small* **6**(5), 695–699 (2010).
12. M. Schierhorn et al., "Photoelectrochemical performance of CdSe nanorod arrays grown on a transparent conducting substrate," *Nano Lett.* **9**(9), 3262–3267 (2009).
13. L. K. Tan, M. A. S. Chong, and H. Gao, "Free-standing porous anodic alumina templates for atomic layer deposition of highly ordered TiO2 nanotube arrays on various substrates," *J. Phys. Chem. C* **112**(1), 69–73 (2008).
14. T. R. B. Foong, A. Sellinger, and X. Hu, "Origin of the bottlenecks in preparing anodized aluminium oxide (AAO) templates on ITO glass," *ACS Nano* **2**(11), 2250–2256 (2008).
15. C. Robert-Goumet et al., "SEM and XPS studies of nanohole arrays on InP(100) surfaces created by coupling AAO templates and low energy Ar+ ion sputtering," *Surf. Sci.* **603**(19), 2923–2927 (2009).
16. M. Z. Hu et al., "Large-area silica nanotubes with controllable geometry on silicon substrates," *Appl. Surf. Sci.* **255**(6), 3563–3566 (2009).
17. Z. Huang et al., "Extended arrays of vertically aligned sub-10 nm diameter [100] Si nanowires by metal-assisted chemical etching," *Nano Lett.* **8**(9), 3046–3051 (2008).
18. J. Byun et al., "Highly ordered nanoporous alumina on conducting substrates with adhesion enhanced by surface modification: universal templates for ultrahigh-density arrays of nanorods," *Adv. Mater.* **22**(18), 2028–2032 (2010).
19. K. Sengupta et al., "Large-scale ordered plastic nanopillars for quantitative live-cell imaging," *Small* **5**(4), 449–453 (2009).
20. N. Haberkorn, J. S. Gutmann, and P. Theato, "Template-assisted fabrication of freestanding nanorod arrays of a hole-conducting cross-linked triphenylamine derivative: toward ordered bulk-heterojunction solar cells," *ACS Nano* **3**(6), 1415–1422 (2009).
21. S. Aksu et al., "High-throughput nanofabrication of infrared plasmonic nanoantenna arrays for vibrational nanospectroscopy," *Nano Lett.* **10**(7), 2511–2518 (2010).
22. T. Deng et al., "Fabrication of silicon nanopore arrays using a combination of dry and wet etching," *J. Vac. Sci. Technol. B* **30**(6), 061804 (2012).
23. Z. Liu, T. Deng, and J. Chen, "Solid-state nanopore fabrication with conventional process," *ECS Trans.* **52**(1), 1047–1052 (2013).
24. T. Deng et al., "Fabrication of inverted-pyramid silicon nanopore arrays with three-step wet etching," *ECS J. Solid State Sci. Technol.* **2**(11), P419–P422 (2013).
25. M. L. Taylor et al., "Ion beam lithograpy using a nano-aperture," *Nucl. Instrum. Methods Phys. Res. B* **260**(1), 426–430 (2007).

Tao Deng got his combined BS degrees from School of Mechanical Engineering and School of Management in Xi'an Jiaotong University in 2010. After that, he joined professor Zewen Liu's group in Tsinghua University to pursue his PhD degree. Now, he is a visiting PhD student in professor David H. Gracias' lab in Johns Hopkins University. His research interests are nano-fabrication and bioMEMS. So far he has authored 6 refereed journal publications.

Zewen Liu received the BS degree from Department of Physics of University of Science and Technology of China, Hefei China and the PhD degree from University of Paris-Sud, Orsay, France in 1983 and 1997 respectively. From 1997 to 1999, he was a post doctor with the Institute of Microelectronics, Tsinghua University (IMETU), Beijing China. Since 1999 he has been working in IMETU as associate professor and was promoted to full professor in 2007. From 2000 to 2003, he was the vice director of IMETU. His current technical interests include semiconductor process, MEMS for wireless communication and bio-medical applications.

Biographies and photographs of the other authors are not available.