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GUEST EDITORIAL

Special Section Guest Editorial: Control of Integrated Circuit Patterning Variance, Part 5: Pattern Placement, Critical Dimension, and Edge-to-Edge Overlay

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The fifth Special Section on Control of IC Patterning Variance has been completed.

What is here for you?

Here are my impressions and comments:

SEM contour-based dimensional metrology in one pattern layer[1] unavoidably finds its way to appealing in-FAB use cases, generating ever stronger user interest and commercial activity, such as patterning (OPC) model build and validation. Researchers from Siemens Digital Industries Software, TASMIT, and IMEC consolidated their recent work in "Applications of large field of view e-beam metrology to contour-based optical proximity correction modeling." Significant as it is for its broad scope and many technical merits, even this paper does not completely account for new technologies and applications coming up—a proverbial "tip of the iceberg." If you become interested and want to learn more, you can attend SPIE Advanced Lithography & Patterning Conferences and look this up in SPIE Proceedings.

Extending applications of SEM contour-based dimensional metrology to process control and selecting superior patterning methods also enables reducing IC device pattern variation. Consider model-based evaluation by Lucas et al. of EPE variations and lithography process margins, "Enhancing mask synthesis for curvilinear masks in full-chip EUV lithography." More accurate patterning (OPC) models bolster their predictions of lower MEEF, CD and EPE variations, and greater lithography process windows with curvilinear, rather than in conventional (Manhattan), mask synthesis. Massive sampling by accurate contour-based dimensional metrology of device patterns in layouts, on product wafers, would go a long way towards in-line validation of this new synthesis, reducing its risks and accelerating its proliferation.

Progress is also made in overlay control. Long-anticipated SEM-based overlay metrology and, especially, metrology of edge-to-edge overlay in the devices, is finally becoming available.[2,3] Tools, targets, and applications are being refined to improve measurement performance. At the same time, we see the emergence of the electrical property based evaluations, also by e-beam systems, of edge-to-edge overlay, the IC Design Rule that most limits today's patterning technology. Two papers report voltage contrast (VC) based evaluation of edge-to-edge overlay: Strojwas et al., "Efficient metrology for edge placement error and process window characterization using design for inspection methodology" and Carballo et al., "Voltage contrast determination of design rules at the limits of EUV single patterning."

With all the good things here, it is even more exciting to see a potentially explosive new form of VC imaging reported by Fukuda et al., "In situ electrical property quantification of memory devices by modulated electron microscopy." By adjusting the e-beam scan rate to match device charging/charge dissipation time constant, they increased available VC image contrast[3] and enabled in-line observation and process control of devices' threshold voltage and source-drain current variations. As if that were not a great achievement, they also extended the VC inspection

applicability to detecting electrically open (contact hole not open, incomplete etch etc.) contacts to floating circuits.

There is a wealth of new and exciting technology presented here for your learning. I do hope you will enjoy this Part 5.

References

1. F. Weisbuch and K. Jantzen, "Enabling scanning electron microscope contour-based optical proximity correction models," *J. Micro/Nanolithogr., MEMS, MOEMS* **14**(2), 021105 (2015).
2. F. Weisbuch, J. Schatz, and M. Ruhm, "Characterizing interlayer edge placement with SEM contours," *J. Micro/Nanolithogr., MEMS, MOEMS* **18**(2), 021203 (2019).
3. O. Inoue and K. Hasumi, "Review of scanning electron microscope-based overlay measurement beyond 3-nm node device," *J. Micro/Nanolithogr., MEMS, MOEMS* **18**(2), 021206 (2019).